March 2018

SemiHow
Know-How for Semiconductor

HRLD40N04K

40V N-Channel Trench MOSFET

Features

- ❑ High Dense Cell Design, Logic Level
- ❑ Reliable and Rugged
- ❑ Advanced Trench Process Technology
- ❑ 100% UIS Tested, 100% Rg Tested

Key Parameters

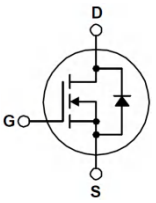
Parameter	Value	Unit
BV_{DSS}	40	V
$I_{D\ (Silicon\ Limited)}$	130	A
$R_{DS(on),\ typ\ @10V}$	3.3	mΩ
$R_{DS(on),\ typ\ @4.5V}$	4.0	mΩ

Application

- ❑ Power Management in Inverter System
- ❑ Synchronous Rectification

Package & Internal Circuit

D-PAK



Absolute Maximum Ratings

T_J=25℃ unless otherwise specified

Symbol	Parameter		Value	Units
V_{DSS}	Drain-Source Voltage		40	V
V_{GS}	Gate-Source Voltage		±20	V
I_D	Drain Current (Silicon Limited)	T_C= 25℃	130	A
		T_C = 100℃	90	A
	Drain Current (Package Limited)	T_C= 25℃	70	A
I_{DM}	Pulsed Drain Current		300	A
E_{AS}	Single Pulsed Avalanche Energy	L=1mH	1050	mJ
P_D	Power Dissipation	T_C = 25℃	115	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	℃

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	1.3	℃/W
$R_{\theta JA}$	Junction-to-Ambient (minimum pad of 2 oz copper)	--	110	℃/W
$R_{\theta JA}$	Junction-to-Ambient (* 1 in^2 pad of 2 oz copper)	--	50	℃/W

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Electrical Characteristics T_J=25 °C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
V_{GS}	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	1.2	--	2.8	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 30 A	--	3.3	4.0	mΩ
		V_{GS} = 4.5 V, I_D = 20 A	--	4.0	4.8	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 30 A	--	90	--	S
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	40	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 32 V, T_J = 125℃	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	--	--	±100	nA
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	5400	--	pF
C_{oss}	Output Capacitance		--	620	--	pF
C_{rss}	Reverse Transfer Capacitance		--	450	--	pF
R_g	Gate Resistance	V_{GS} = 0 V, V_{DS} = 0 V, f = 1MHz	--	1.5	--	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	V_{DS} = 20 V, I_D = 30 A, R_G = 6 Ω	--	40	--	ns
t_r	Turn-On Rise Time		--	60	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	220	--	ns
t_f	Turn-Off Fall Time		--	50	--	ns
$Q_{g\ (10V)}$	Total Gate Charge	V_{DS} = 32 V, I_D = 30 A, V_{GS} = 10 V	--	130	--	nC
$Q_{g\ (4.5V)}$	Total Gate Charge		--	67	--	nC
Q_{gs}	Gate-Source Charge		--	20	--	nC
Q_{gd}	Gate-Drain Charge		--	35	--	nC
Source-Drain Diode Characteristics						
V_{SD}	Source-Drain Diode Forward Voltage	I_S = 30 A, V_{GS} = 0 V	--	--	1.3	V
trr	Reverse Recovery Time	I_S = 30 A, V_{GS} = 0 V, di_F/dt = 100 A/μs	--	160	--	ns
Qrr	Reverse Recovery Charge		--	160	--	nC

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Typical Characteristics

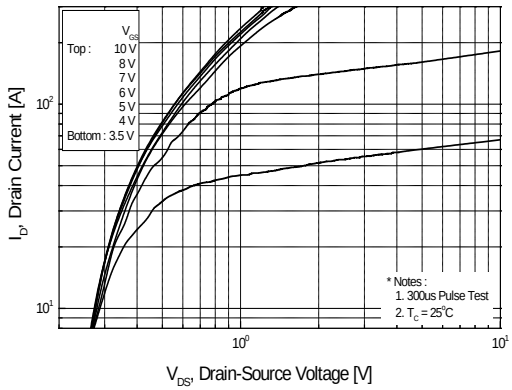

Figure 1. On Region Characteristics

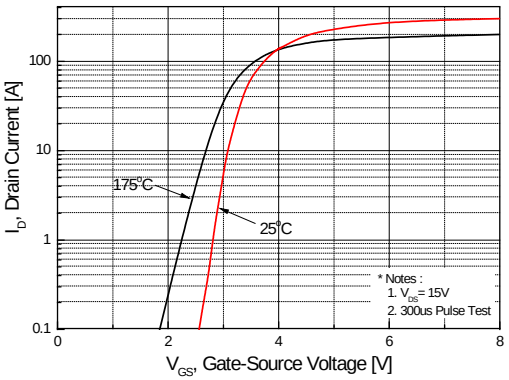

Figure 2. Transfer Characteristics

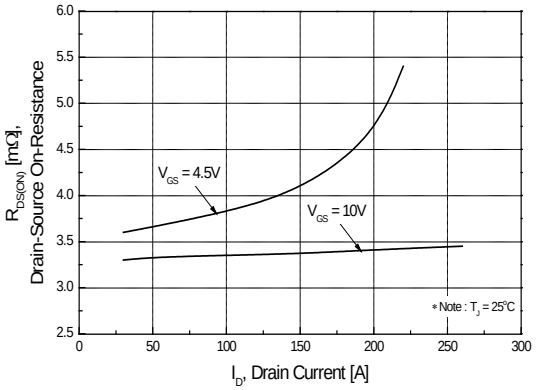

Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

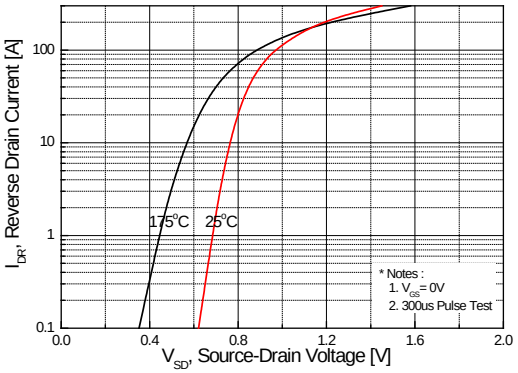

Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

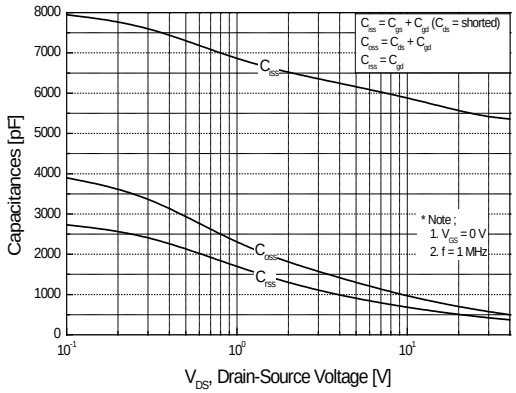

Figure 5. Capacitance Characteristics

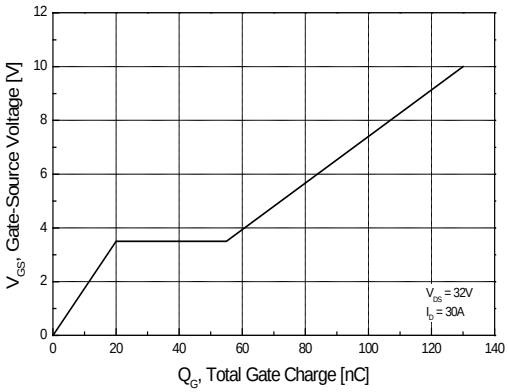

Figure 6. Gate Charge Characteristics

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Typical Characteristics (continued)

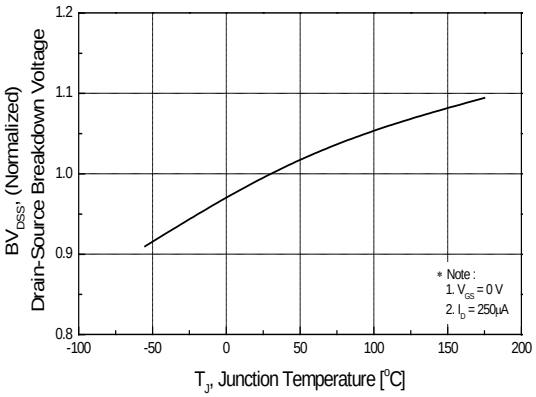

Figure 7. On-Resistance Variation vs Gate-Source Voltage

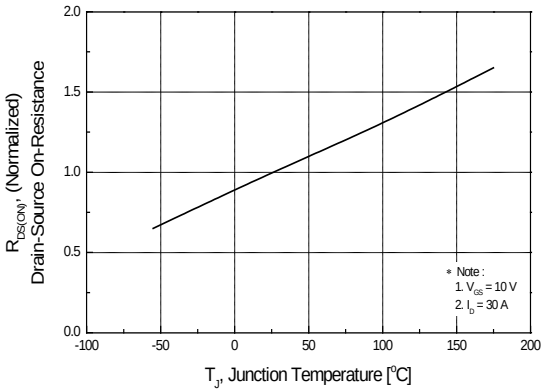

Figure 8. On-Resistance Variation vs Temperature

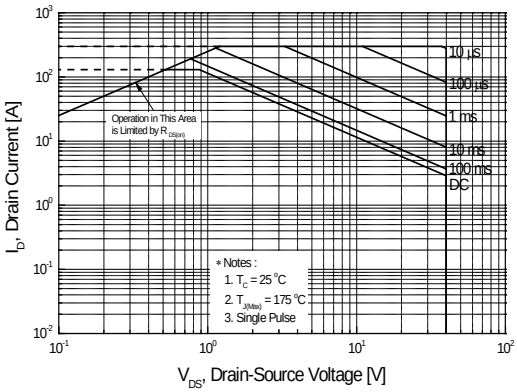

Figure 9. Maximum Safe Operating Area

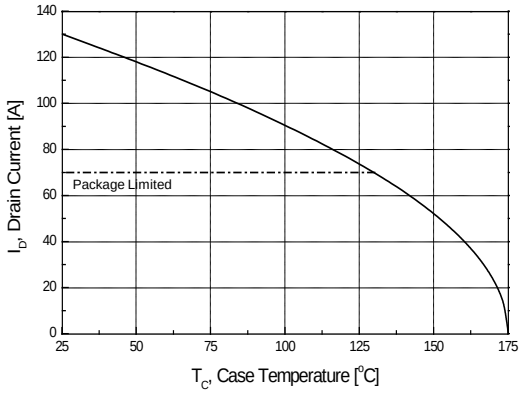

Figure 10. Maximum Drain Current vs Case Temperature

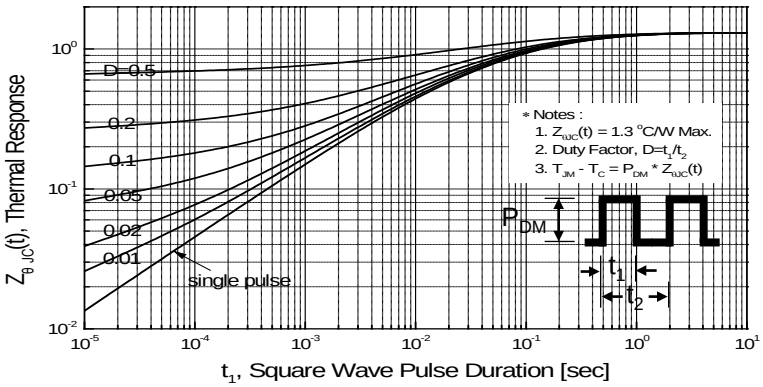

Figure 11. Transient Thermal Response Curve

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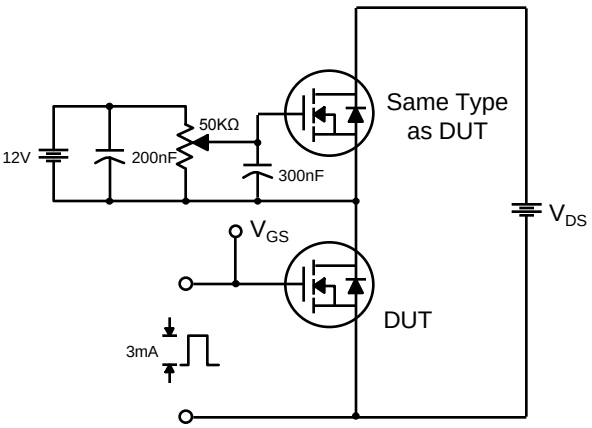
Fig 12. Gate Charge Test Circuit & Waveform



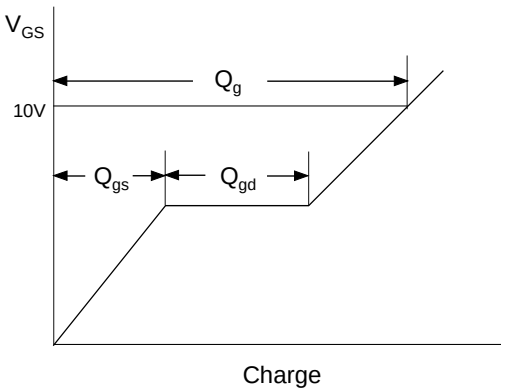
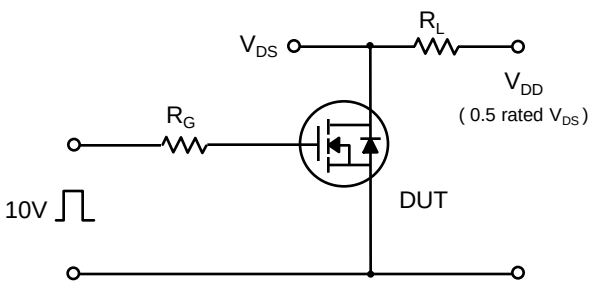


Fig 13. Resistive Switching Test Circuit & Waveforms



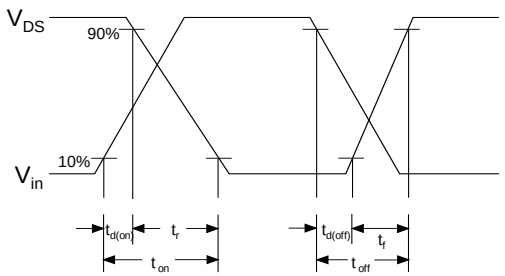
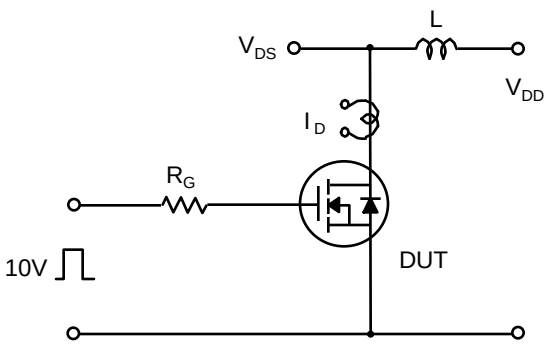


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms



$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

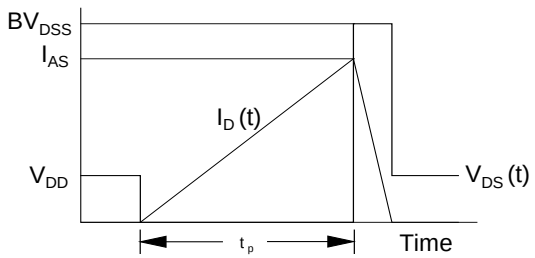


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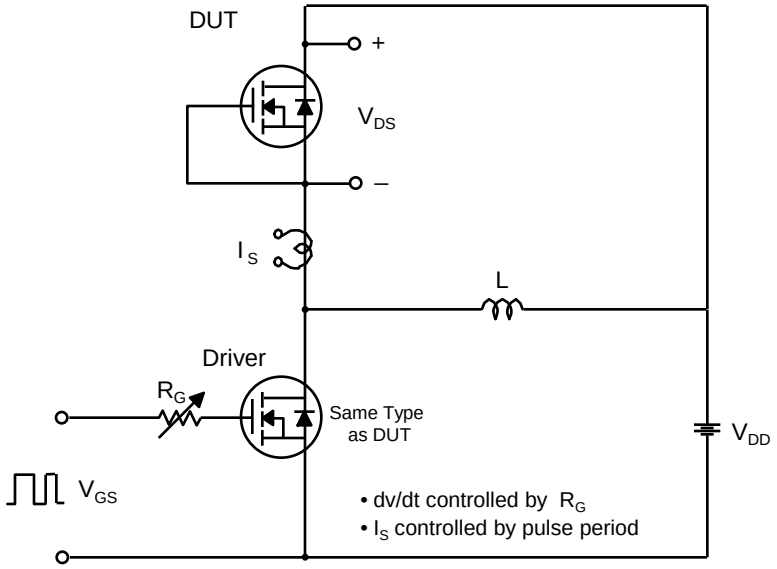
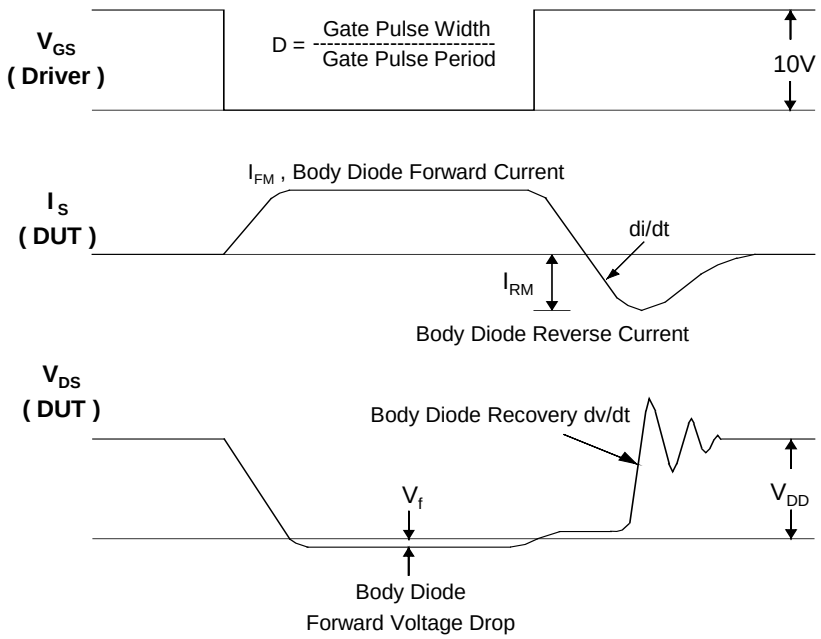
Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms





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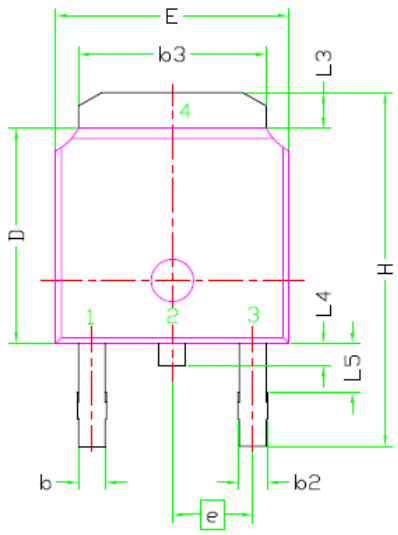
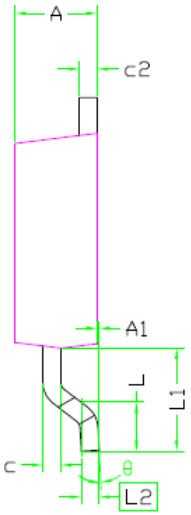
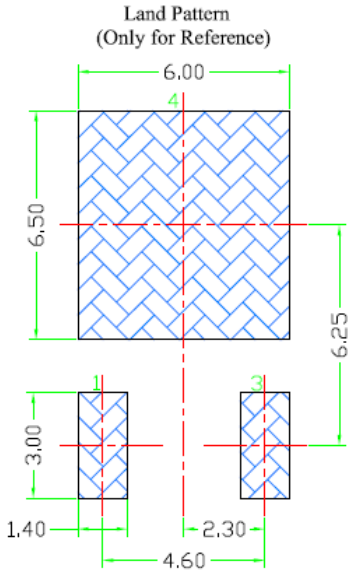
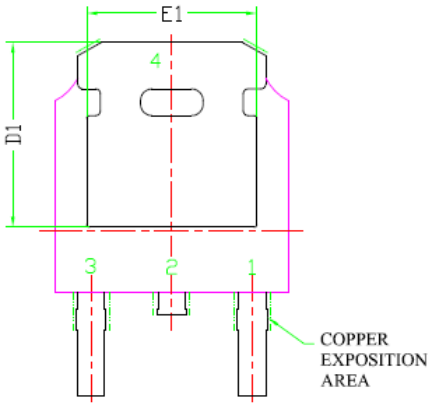
Package Dimension

D-PAK
(TO-252A)









SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
E	6.40	6.60	6.731
L	1.40	1.52	1.77
L1	2.743 REF		
L2	0.508 BSC		
L3	0.89	--	1.27
L4	0.64	--	1.01
L5	--	--	--
D	6.00	6.10	6.223
H	9.40	10.00	10.40
b	0.64	0.76	0.88
b2	0.77	0.84	1.14
b3	5.21	5.34	5.46
e	2.286 BSC		
A	2.20	2.30	2.38
A1	0	--	0.127
c	0.45	0.50	0.60
c2	0.45	0.50	0.58
D1	5.21	--	--
E1	4.40	--	--
θ	0°	--	10°

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