Sep 2015

SemiHow
Know-How for Semiconductor

BV_{DSS} = 100 V

$R_{DS(on)\ typ}$ = 10 mΩ

I_D = 73 A

HRD120N10K / HRU120N10K
100V N-Channel Trench MOSFET

FEATURES

❑ Originative New Design
❑ Superior Avalanche Rugged Technology
❑ Excellent Switching Characteristics
❑ Unrivalled Gate Charge : 65 nC (Typ.)
❑ Extended Safe Operating Area
❑ Lower $R_{DS(ON)}$: 10 mΩ (Typ.) @V_{GS}=10V
❑ 100% Avalanche Tested

D-PAK **I-PAK**

HRD120N10K **HRU120N10K**

1.Gate 2. Drain 3. Source
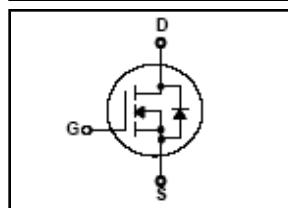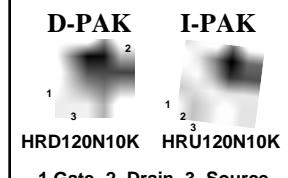
Absolute Maximum Ratings T_C=25℃ unless otherwise specified

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source Voltage	100	V
I_D	Drain Current – Continuous (T_C = 25℃)	73 *	A
	Drain Current – Continuous (T_C = 100℃)	51 *	A
I_{DM}	Drain Current – Pulsed (Note 1)	200 *	A
V_{GS}	Gate-Source Voltage	±25	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	265	mJ
E_{AR}	Repetitive Avalanche Energy (Note 1)	11	mJ
P_D	Power Dissipation (T_A = 25℃)*	3	W
	Power Dissipation (T_C = 25℃)	110	W
	- Derate above 25℃	0.73	W/℃
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	℃
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	℃

* Drain current limited by maximum junction temperature

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{θJC}$	Junction-to-Case	--	1.4	℃/W
$R_{θJA}$	Junction-to-Ambient*	--	50	
$R_{θJA}$	Junction-to-Ambient	--	110	

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics T_J=25 °C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
V_{GS}	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	2.0	--	3.6	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10$ V, $I_D = 40$ A	--	10	12	mΩ
g_{FS}	Forward Transconductance	$V_{DS} = 20$, $I_D = 40$ A	--	70	--	S
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250 \mu A$	100	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80$ V, $V_{GS} = 0$ V	--	--	1	μA
		$V_{DS} = 80$ V, $T_J = 125℃$	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 25$ V, $V_{DS} = 0$ V	--	--	± 100	nA
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25$ V, $V_{GS} = 0$ V, f = 1.0 MHz	--	3150	--	pF
C_{oss}	Output Capacitance		--	340	--	pF
C_{rss}	Reverse Transfer Capacitance		--	180	--	pF
R_g	Gate Resistance	$V_{GS} = 0$ V, $V_{DS} = 0$ V, f = 1MHz	--	1.2	--	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	$V_{DS} = 50$ V, $I_D = 30$ A, $R_G = 6$ Ω	--	40	--	ns
t_r	Turn-On Rise Time		--	50	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	120	--	ns
t_f	Turn-Off Fall Time		--	40	--	ns
Q_g	Total Gate Charge	$V_{DS} = 80$ V, $I_D = 30$ A, $V_{GS} = 10$ V	--	65	--	nC
Q_{gs}	Gate-Source Charge		--	12	--	nC
Q_{gd}	Gate-Drain Charge		--	24	--	nC
Source-Drain Diode Maximum Ratings and Characteristics						
I_S	Continuous Source-Drain Diode Forward Current		--	--	73	A
I_{SM}	Pulsed Source-Drain Diode Forward Current		--	--	200	
V_{SD}	Source-Drain Diode Forward Voltage	$I_S = 30$ A, $V_{GS} = 0$ V	--	--	1.3	V
trr	Reverse Recovery Time	$I_S = 30$ A, $V_{GS} = 0$ V, $di_F/dt = 100$ A/μs	--	50	--	ns
Qrr	Reverse Recovery Charge		--	80	--	nC

Notes :
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L=1mH, I_{AS}=20A, V_{DD}=25V, R_G=25Ω, Starting T_J =25°C

Typical Characteristics
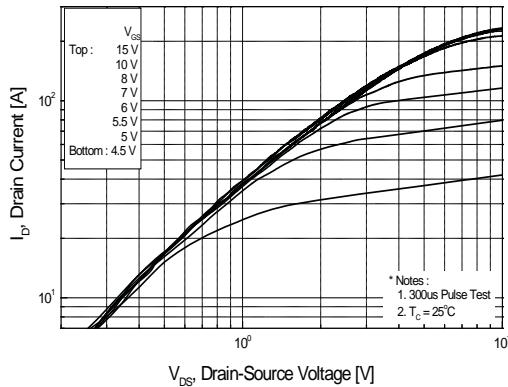

Figure 1. On Region Characteristics
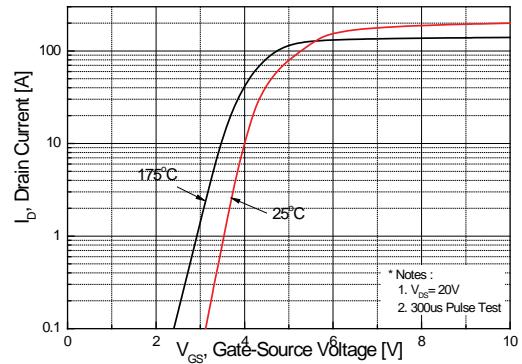
**Figure 2. Transfer Characteristics**
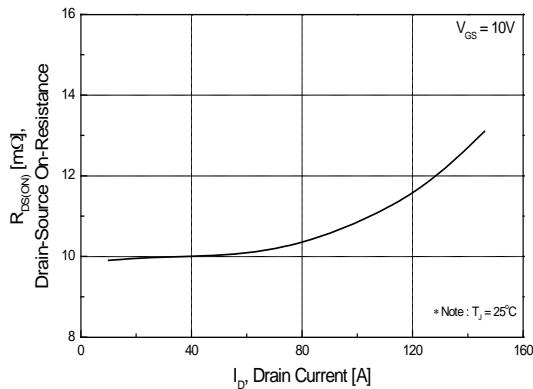
**Figure 3. On Resistance Variation vs Drain Current and Gate Voltage**
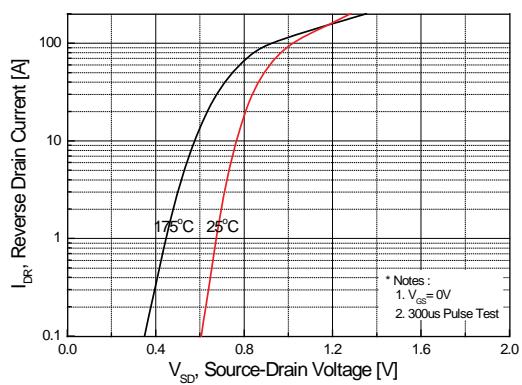
**Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature**
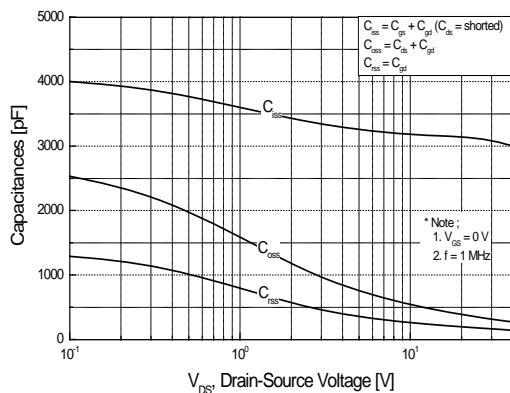

Figure 5. Capacitance Characteristics
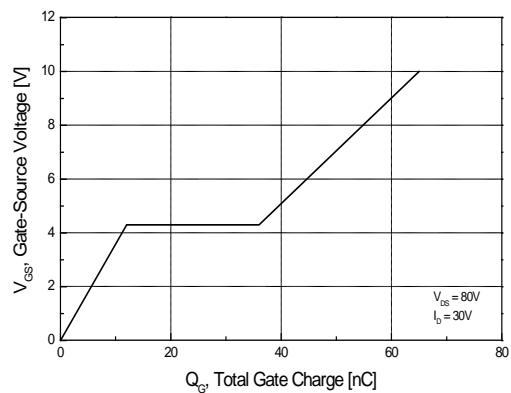
Figure 6. Gate Charge Characteristics

Typical Characteristics   (continued)
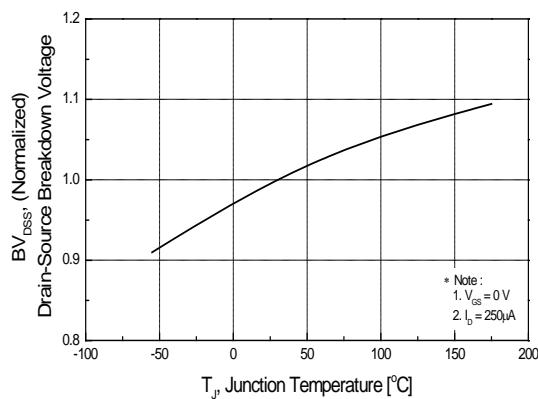

**Figure 7. Breakdown Voltage Variation
vs Temperature**
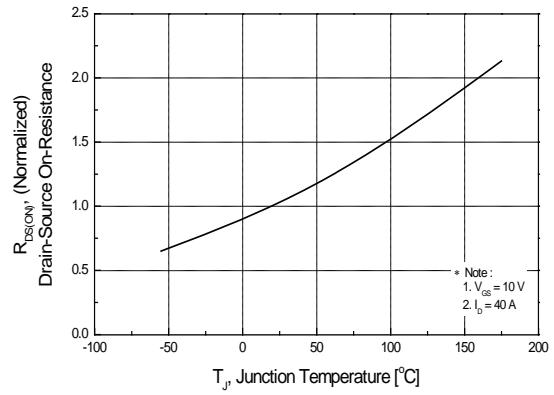

**Figure 8. On-Resistance Variation
vs Temperature**
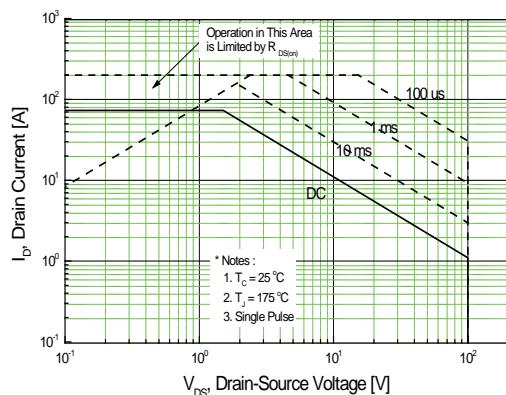

Figure 9. Maximum Safe Operating Area
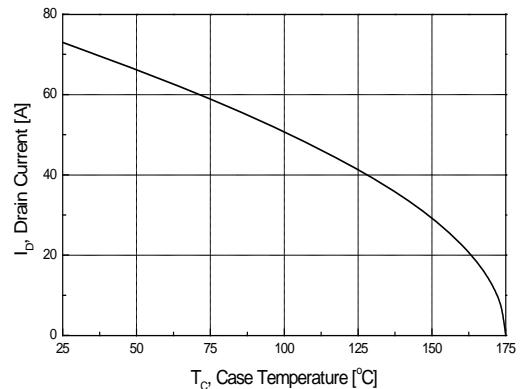

**Figure 10. Maximum Drain Current
vs Case Temperature**
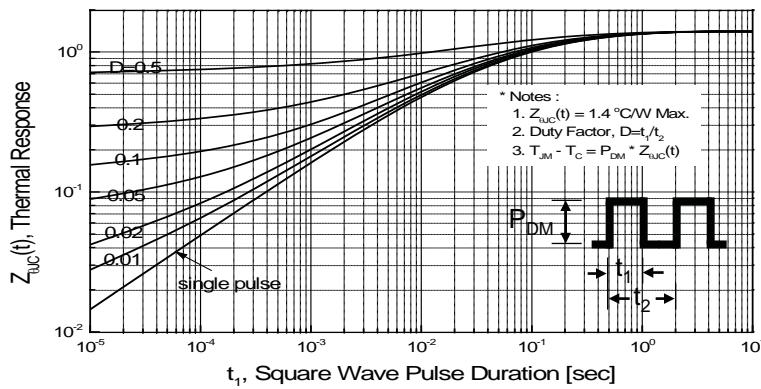
Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform

Same Type
as DUT

DUT

Charge
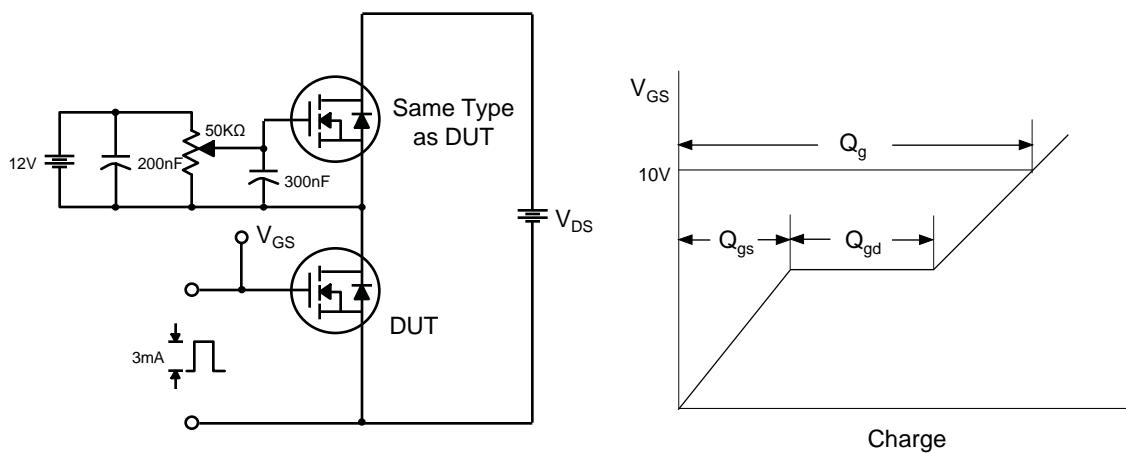
Fig 13. Resistive Switching Test Circuit & Waveforms

DUT

**Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms**

$$E_{AS} = \frac{1}{2} \ L_L I_{AS}^2 \ \frac{BV_{DSS}}{BV_{DSS} -- V_{DD}}$$

DUT
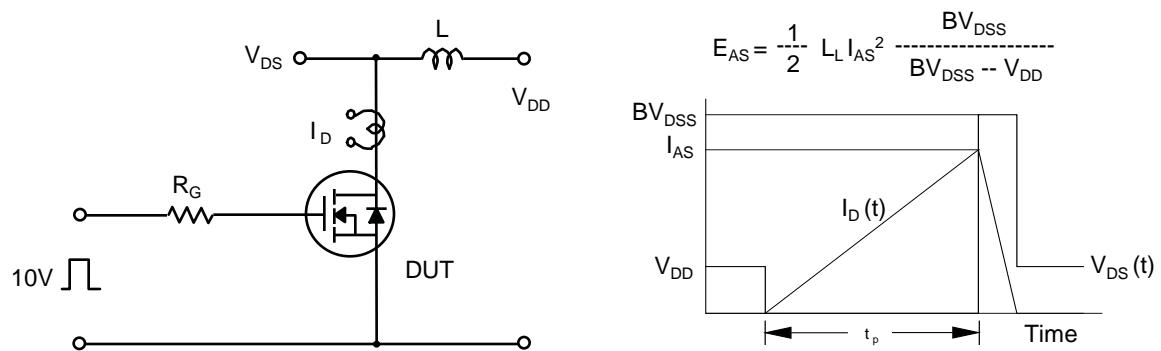
Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$
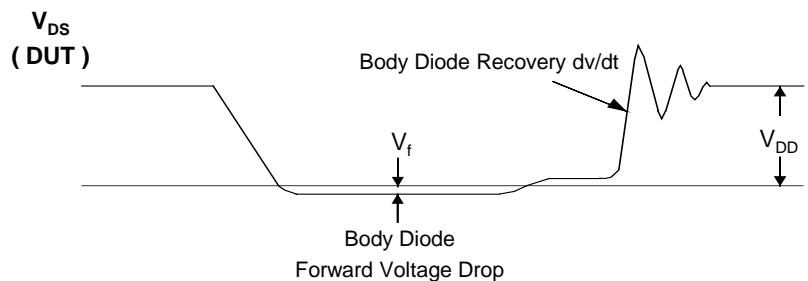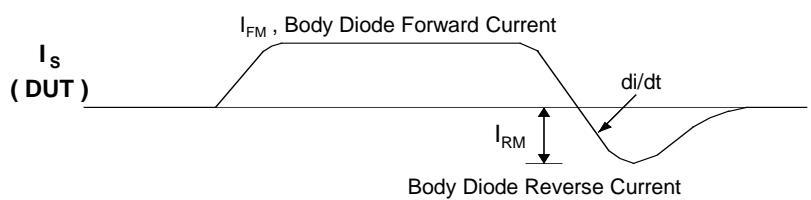
Package Dimension

D-PAK
(TO-252A)

A-A
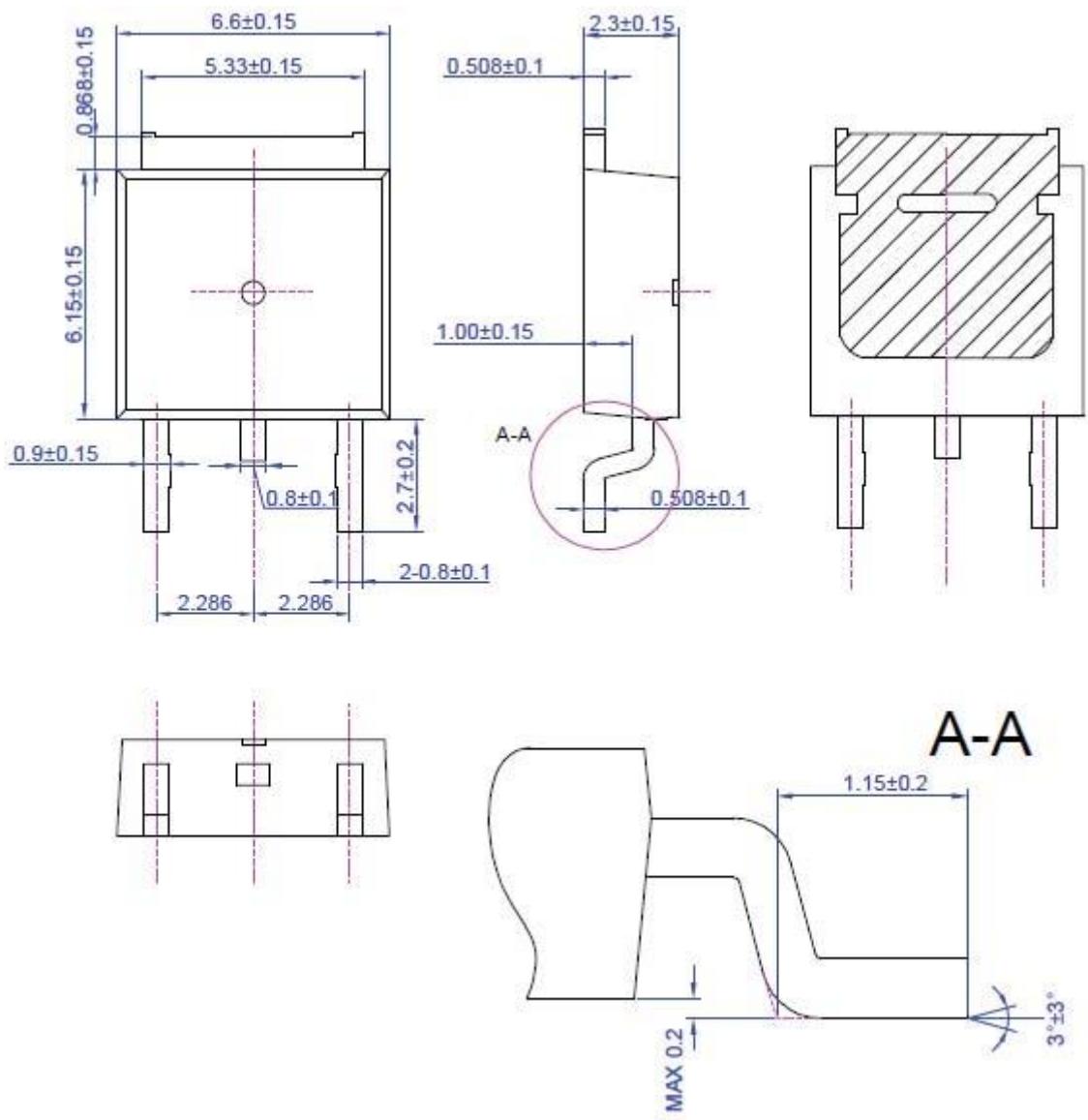
Package Dimension

I–PAK
(TO–251A)