



HRLT1B0N10K

100V N-Channel Trench MOSFET

Features

- ESD Protect
- Reliable and Rugged
- High Density Cell Design for Ultra Low $R_{DS(on)}$
- 100% Avalanche Tested
- RoHS Compliant

Key Parameters

Parameter	Value	Unit
BV_{DSS}	100	V
I_D	3.5	A
$R_{DS(on)}$, typ @10V	85	m Ω
$R_{DS(on)}$, typ @4.5V	100	m Ω

SOT-223



Symbol



Absolute Maximum Ratings $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Unit	
V_{DSS}	Drain-Source Voltage	100	V	
V_{GS}	Gate-Source Voltage	± 20	V	
I_D	Drain Current	$T_A = 25^\circ\text{C}$	3.5	A
		$T_A = 70^\circ\text{C}$	2.8	A
I_{DM}	Pulsed Drain Current	14	A	
E_{AS}	Single Pulsed Avalanche Energy	L=1mH	21	mJ
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	2.1	W
		$T_A = 70^\circ\text{C}$	1.3	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$	

Thermal Resistance Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Junction-to-Ambient (1 in ² pad of 2 oz copper), Max.	60	$^\circ\text{C}/\text{W}$

Electrical Characteristics $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
On Characteristics						
V_{GS}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.5	--	2.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\ \text{V}, I_D = 3.5\ \text{A}$	--	85	105	m Ω
		$V_{GS} = 4.5\ \text{V}, I_D = 2.0\ \text{A}$	--	100	140	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 5\ \text{V}, I_D = 3.5\ \text{A}$	--	12	--	S
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\ \text{V}, I_D = 250\ \mu\text{A}$	100	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\ \text{V}, V_{GS} = 0$	--	--	1	μA
		$V_{DS} = 80\ \text{V}, T_J = 85^\circ\text{C}$	--	--	30	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 16\ \text{V}, V_{DS} = 0\ \text{V}$	--	--	± 10	μA
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 50\ \text{V}, V_{GS} = 0\ \text{V},$ $f = 1.0\ \text{MHz}$	--	970	--	pF
C_{oss}	Output Capacitance		--	52	--	pF
C_{rss}	Reverse Transfer Capacitance		--	32	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	$V_{DS} = 50\ \text{V}, I_D = 3.5\ \text{A},$ $R_G = 25\ \Omega$ (Note 2,3)	--	17	--	ns
t_r	Turn-On Rise Time		--	24	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	85	--	ns
t_f	Turn-Off Fall Time		--	12	--	ns
$Q_{g(10V)}$	Total Gate Charge	$V_{DS} = 80\ \text{V}, I_D = 3.5\ \text{A},$ $V_{GS} = 10\ \text{V}$ (Note 2,3)	--	20	26	nC
$Q_{g(4.5V)}$	Total Gate Charge		--	10	--	nC
Q_{gs}	Gate-Source Charge		--	3.0	--	nC
Q_{gd}	Gate-Drain Charge		--	4.2	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	3.5	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	14	A
V_{SD}	Drain-Source Diode Forward Voltage	$I_S = 3.5\ \text{A}, V_{GS} = 0\ \text{V}$	--	--	1.1	V
t_{rr}	Reverse Recovery Time	$I_S = 3.5\ \text{A}, di_f/dt = 100\ \text{A}/\mu\text{s}$	--	36	--	ns
Q_{rr}	Reverse Recovery Charge		--	50	--	nC

Notes :

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. Pulse Test : Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$
3. Essentially Independent of Operating Temperature

Typical Characteristics

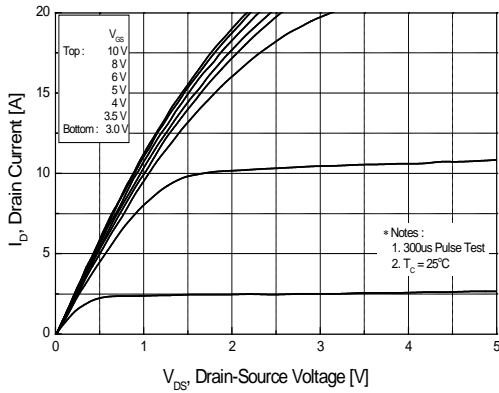


Figure 1. On Region Characteristics

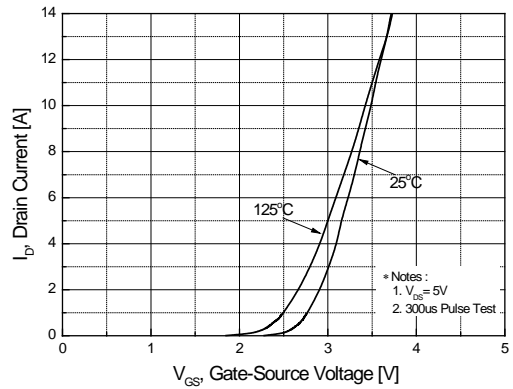


Figure 2. Transfer Characteristics

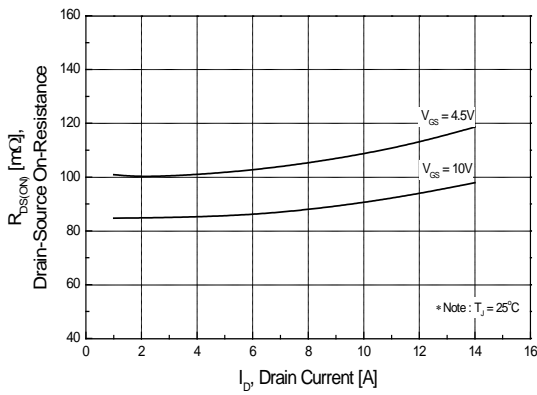


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

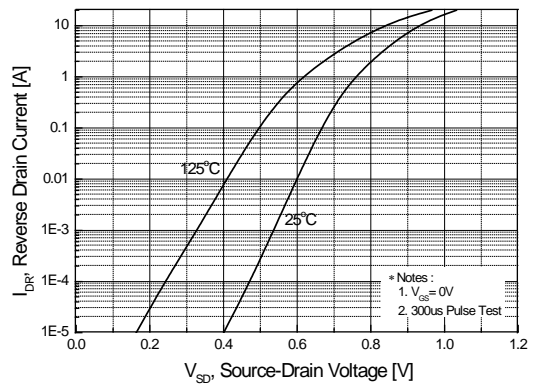


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

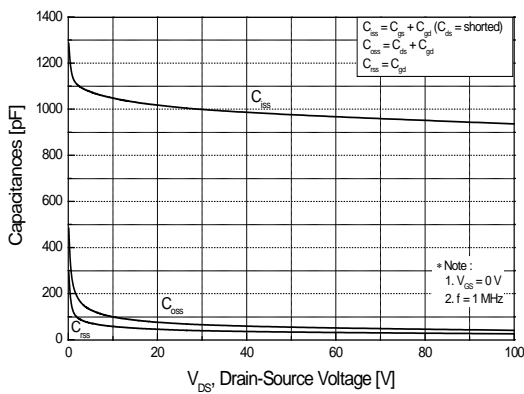


Figure 5. Capacitance Characteristics

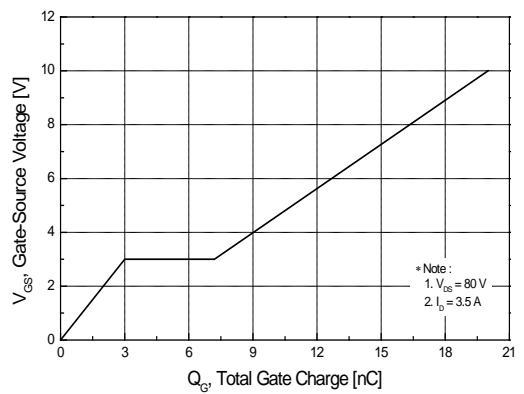


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

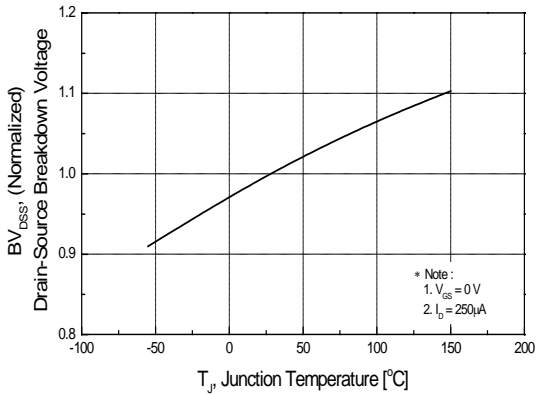


Figure 7. Breakdown Voltage Variation vs Temperature

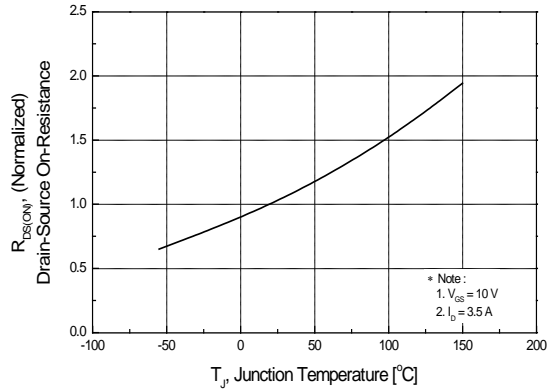


Figure 8. On-Resistance Variation vs Temperature

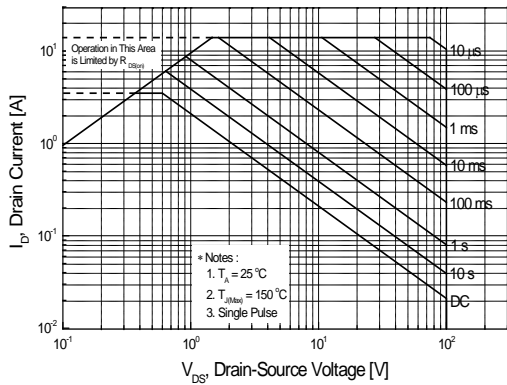


Figure 9. Maximum Safe Operating Area

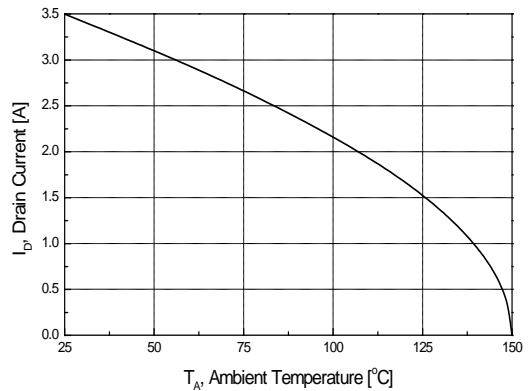


Figure 10. Maximum Drain Current vs Case Temperature

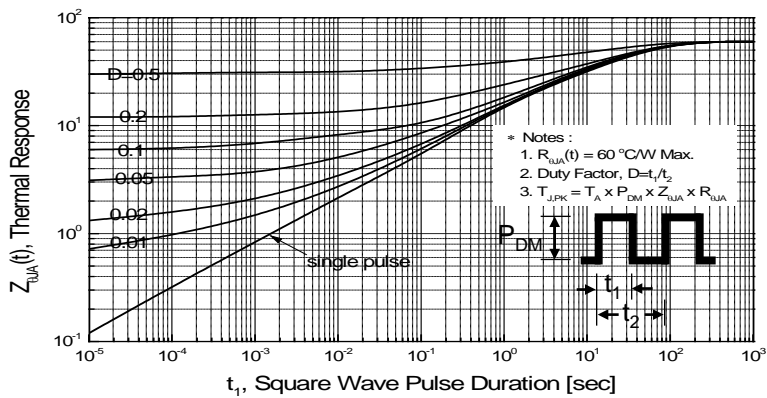


Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform



Fig 13. Resistive Switching Test Circuit & Waveforms

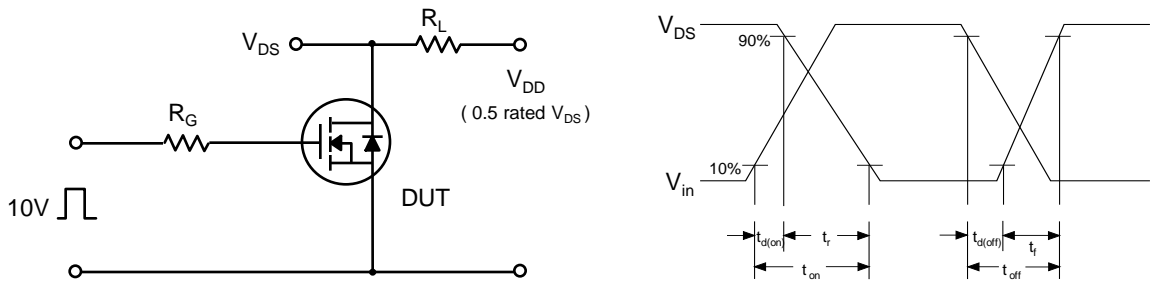


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

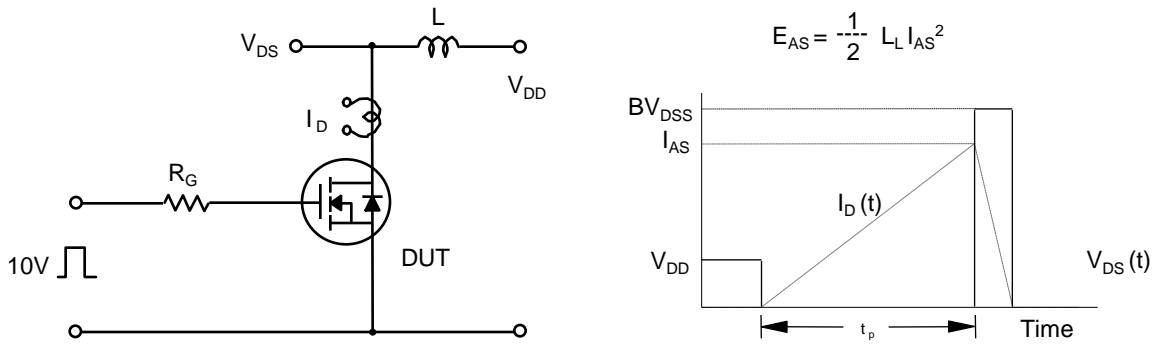
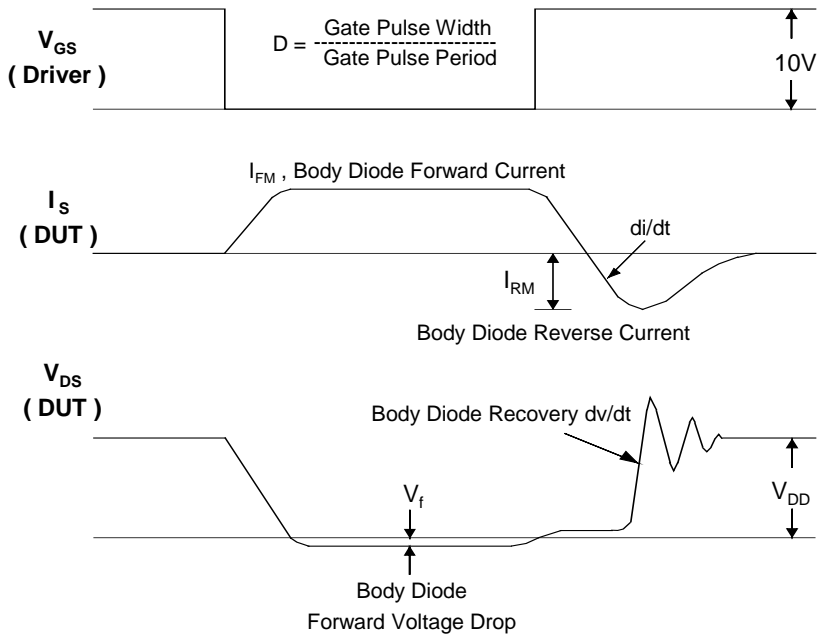
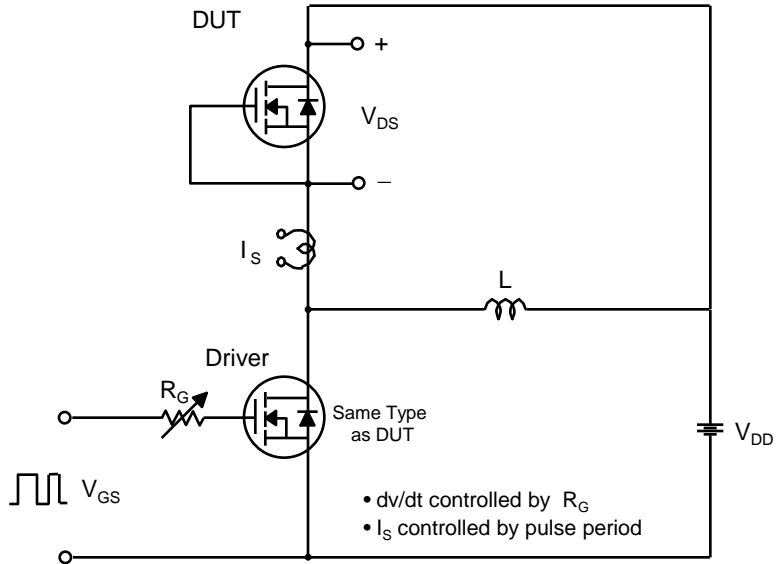
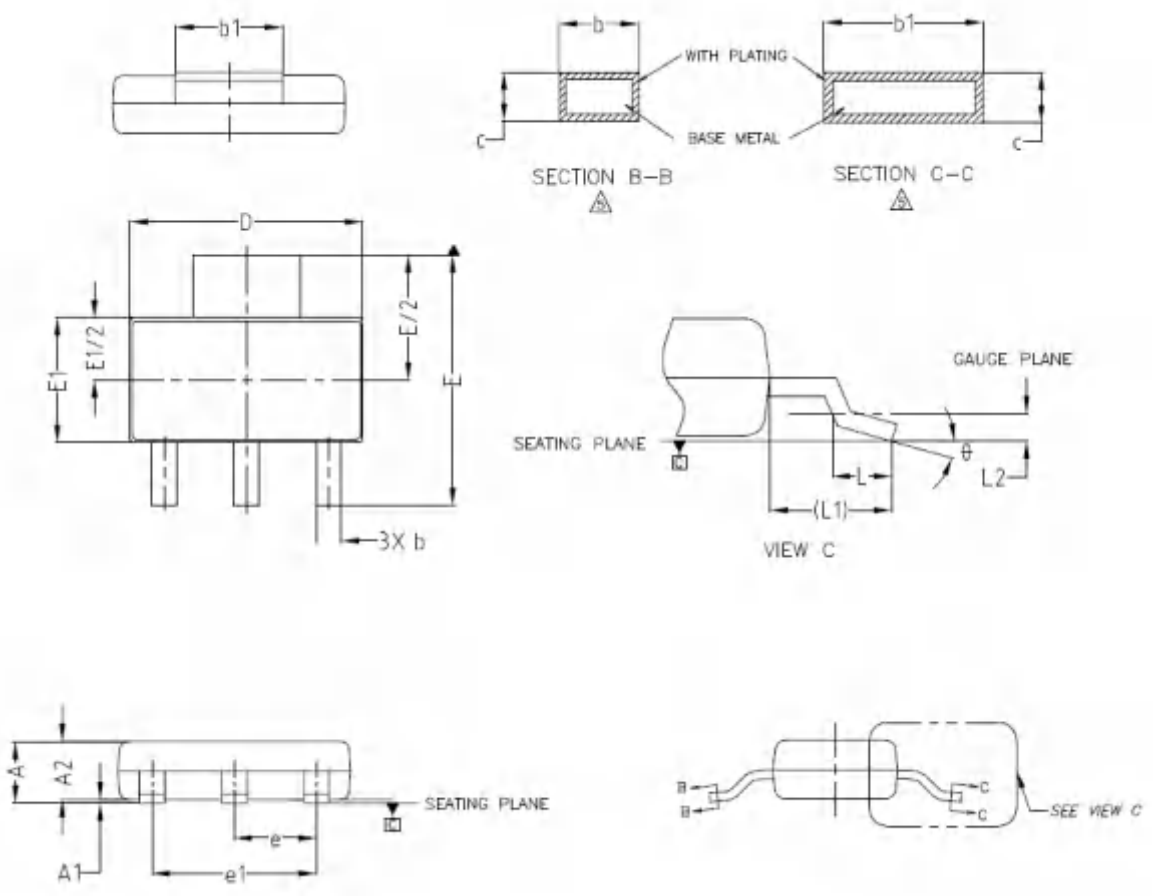


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimension

SOT-223



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	—	—	1.50	
A1	10.00	—	11.10	
A2	1.80	1.85	1.90	
b	0.68	—	0.76	5
b1	2.95	—	3.07	5
c	0.25	—	0.38	5
D	6.40	6.50	6.60	1,3
E	10.80	7.00	7.30	
E1	3.40	3.50	3.60	2,3
e	2.30 BSC			
e1	4.60 BSC			
L	0.15	—	0.65	
L1	1.75 REF			
L2	0.10 BSC			
B	0	—	10	
B'	5°	—	10°	