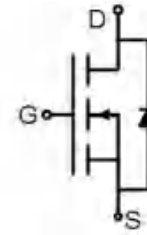


# APG035N04Q

## N-Channel Enhancement Mosfet

### Feature

- 40V,70A  
 $R_{DS(ON)} < 3.2m\Omega @ V_{GS}=10V$  (TYP:2.8m $\Omega$ )  
 $R_{DS(ON)} < 5.2m\Omega @ V_{GS}=4.5V$  (TYP:4.4m $\Omega$ )
- Split Gate Trench Technology
- Lead free product is acquired
- Excellent  $R_{DS(ON)}$  and Low Gate Charge



Schematic Diagram

### Application

- PWM applications
- Load Switch
- Power management



Marking and pin Assignment

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
G035N04	APG035N04Q	PDFN3X3-8L	13 inch	-	5000

### ABSOLUTE MAXIMUM RATINGS ( $T_a=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current ( $T_a = 25^{\circ}C$ )	$I_D$	70	A
Continuous Drain Current ( $T_a = 100^{\circ}C$ )	$I_D$	51	A
Pulsed Drain Current <sup>(1)</sup>	$I_{DM}$	280	A
Single Pulsed Avalanche Energy <sup>(2)</sup>	$E_{AS}$	76	mJ
Power Dissipation	$P_D$	40	W
Thermal Resistance from Junction to Case	$R_{\theta JC}$	3.1	$^{\circ}C/W$
Junction Temperature	$T_J$	150	$^{\circ}C$
Storage Temperature	$T_{STG}$	-55~ +150	$^{\circ}C$

### MOSFET ELECTRICAL CHARACTERISTICS(T<sub>a</sub>=25°C unless otherwise noted)

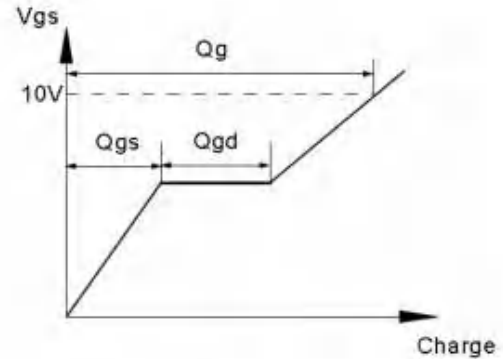
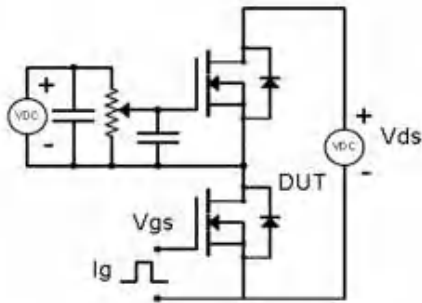
Parameter	Symbol	Test Condition	Min	Type	Max	Unit
<b>Static Characteristics</b>						
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	40	-	-	V
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> =40V, V <sub>GS</sub> = 0V	-	-	1	μA
Gate-body leakage current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> = 0V	-	-	±100	nA
Gate threshold voltage <sup>(3)</sup>	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	1.7	2.2	V
Drain-source on-resistance <sup>(3)</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	2.8	3.5	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =15A	-	4.4	5.2	
Gate Resistance	R <sub>g</sub>	V <sub>DS</sub> =V <sub>GS</sub> =0V, f =1MHz	-	8.4	-	Ω
<b>Dynamic characteristics</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, f =1MHz	-	1280	-	pF
Output Capacitance	C <sub>oss</sub>		-	426	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	30	-	
<b>Switching characteristics</b>						
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> =20V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V, R <sub>G</sub> =6Ω	-	7	-	ns
Turn-on rise time	t <sub>r</sub>		-	6.5	-	
Turn-off delay time	t <sub>d(off)</sub>		-	29	-	
Turn-off fall time	t <sub>f</sub>		-	13	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =20V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V	-	20.3	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	3.9	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	4.2	-	
Reverse Recovery Chrage	Q <sub>rr</sub>	I <sub>F</sub> =15A, di/dt=100A/us		17		nC
Reverse Recovery Time	T <sub>rr</sub>	I <sub>F</sub> =15A, di/dt=100A/us		30		ns
<b>Source-Drain Diode characteristics</b>						
Diode Forward voltage <sup>(3)</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =50A	-	-	1.2	V
Diode Forward current <sup>(4)</sup>	I <sub>S</sub>		-	-	70	A

#### Notes:

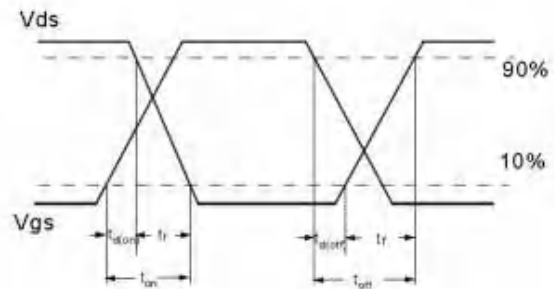
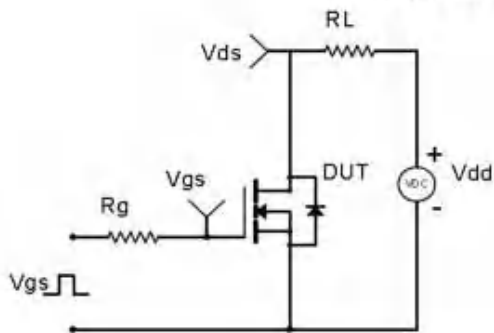
1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition: T<sub>J</sub>=25°C, V<sub>DD</sub>=20V, R<sub>G</sub>=50 Ω, L=0.5Mh, I<sub>AS</sub>=17.5A
3. Pulse Test: pulse width≤300μs, duty cycle≤2%
4. Surface Mounted on FR4 Board, t≤10 sec

**Test Circuit & Waveform**

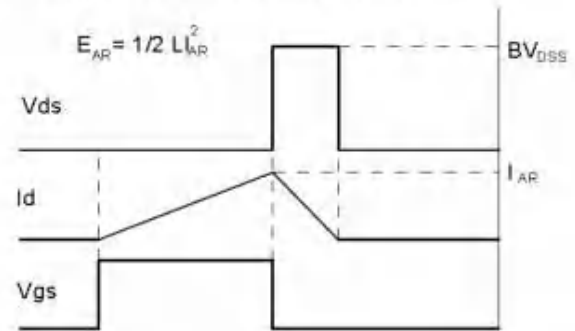
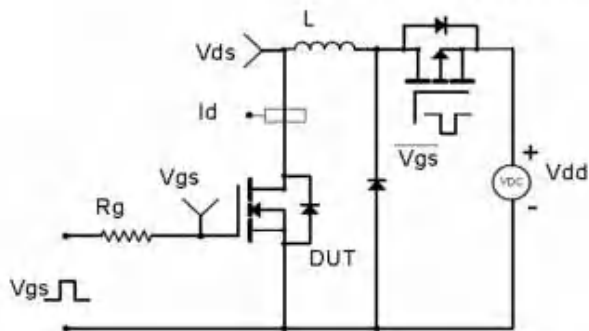
Gate Charge Test Circuit & Waveform



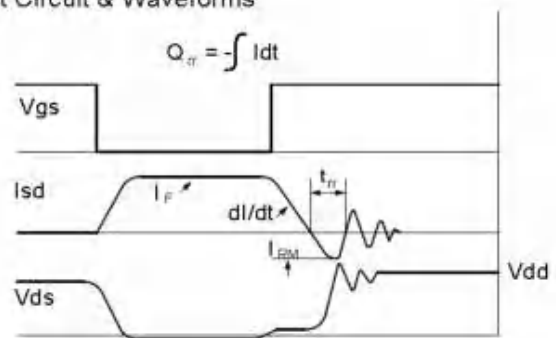
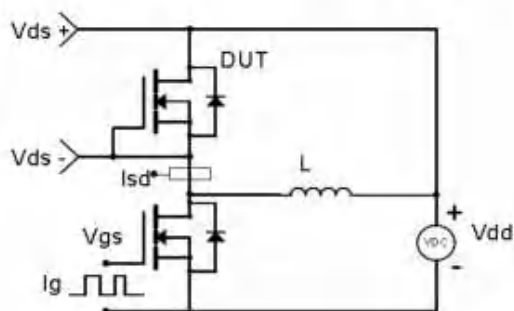
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



**Electrical Characteristics Diagrams**

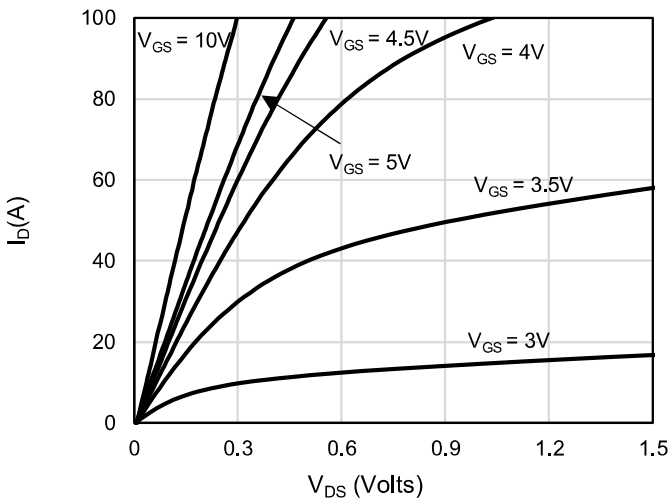


Figure 1: On-Region Characteristics

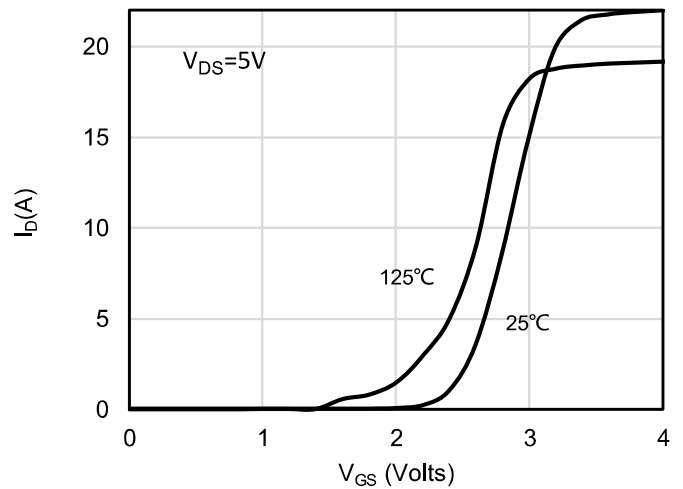


Figure 2: Transfer Characteristics

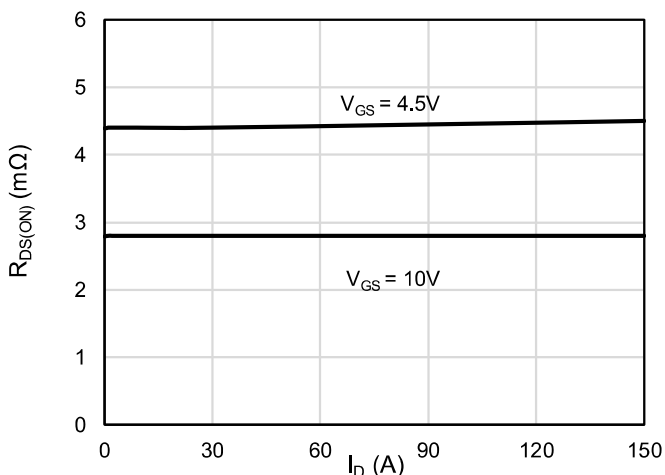


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

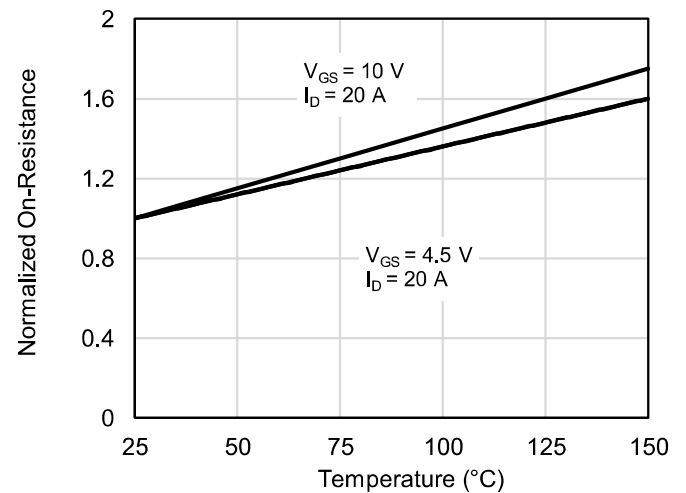


Figure 4: On-Resistance vs. Junction Temperature

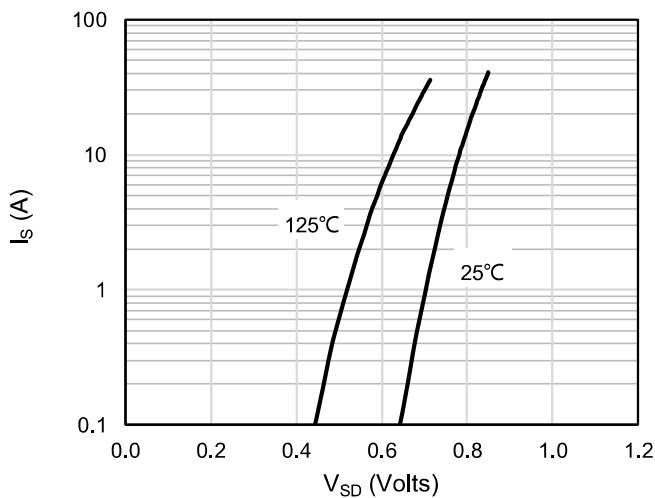


Figure 5: Body-Diode Characteristics

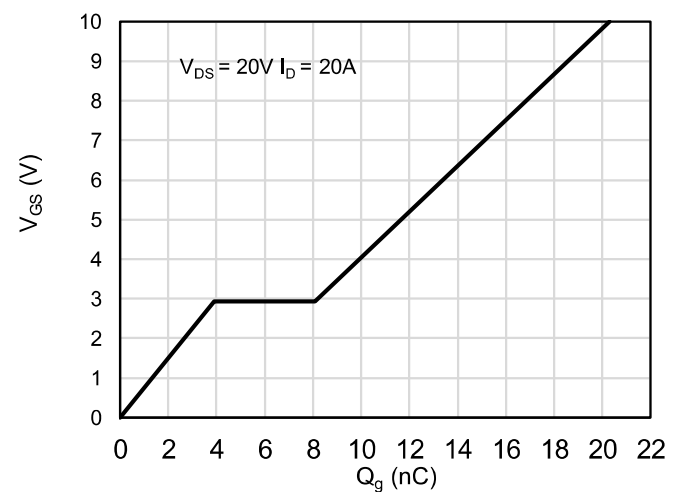


Figure 6: Gate-Charge Characteristics

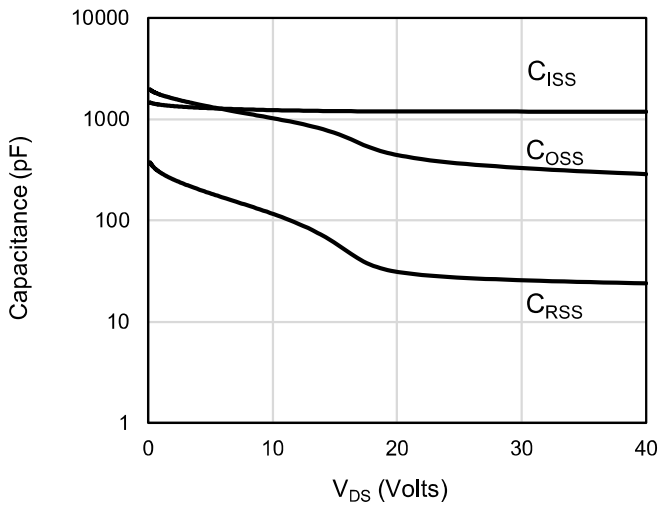


Figure 7: Capacitance Characteristics

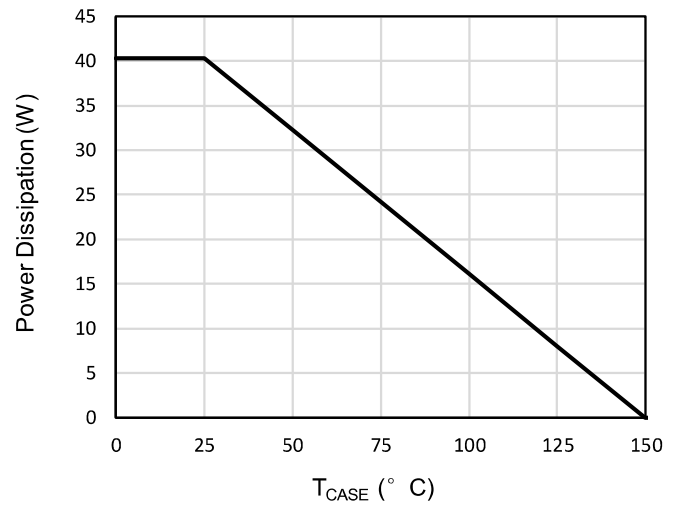


Figure 8: Power De-rating

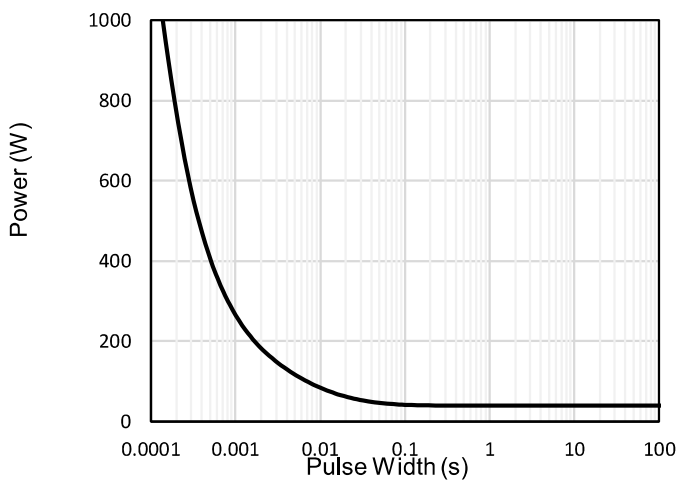


Figure 9: Single Pulse Power Rating Junction-to-Case

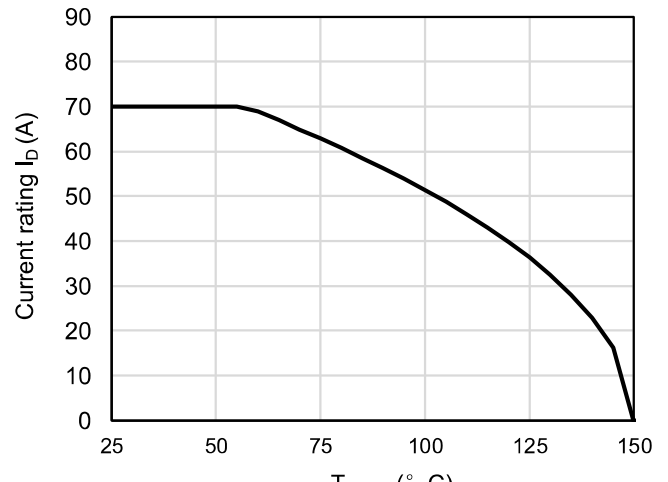


Figure 10: Current De-rating

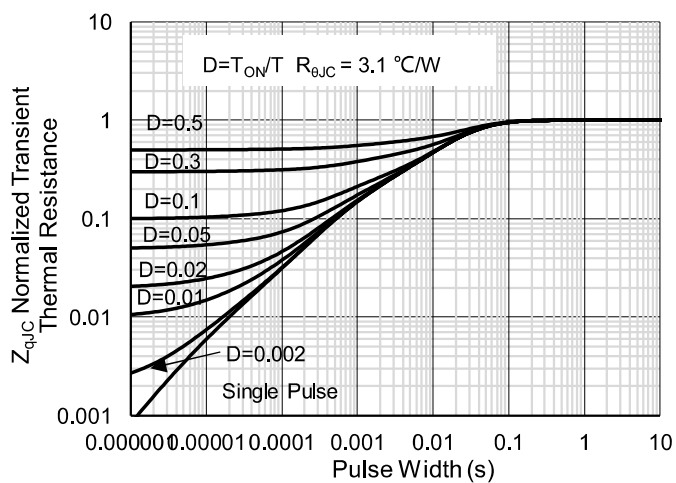


Figure 11: Normalized Maximum Transient Thermal Impedance

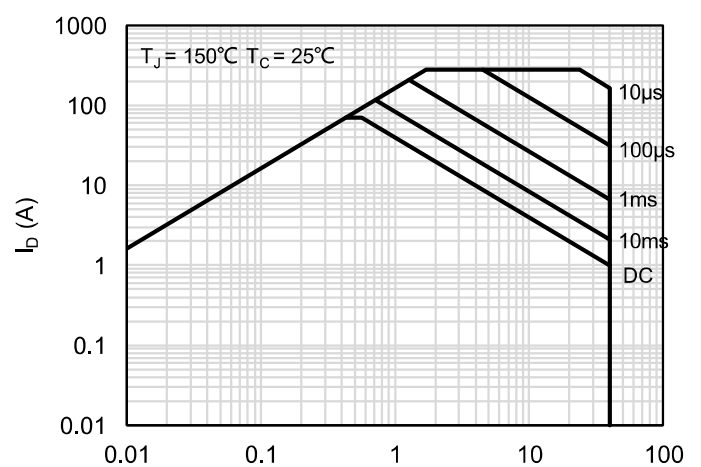
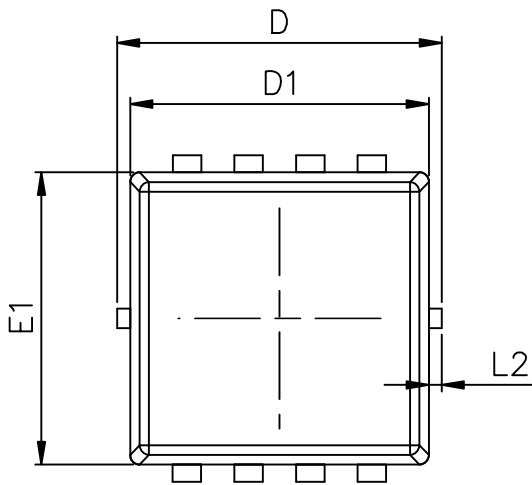
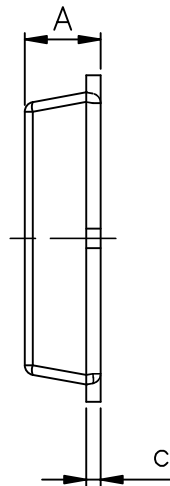


Figure 12: Maximum Forward Biased Safe Operating Area

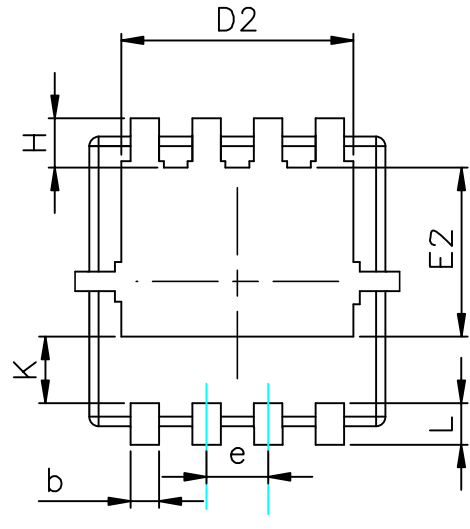
**Package Outlines**



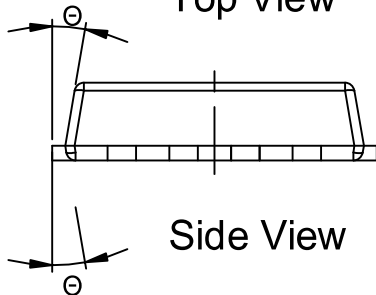
Top View



Side View



Bottom View



Side View

SYMBOL	MIN	NOM	MAX
A	0.70	0.80	0.90
b	0.20	0.30	0.40
c	0.14	0.15	0.25
D	3.20	3.30	3.40
D1	3.00	3.15	3.30
D2	2.35	2.45	2.55
e	0.65 BSC		
E	3.25	3.35	3.45
E1	2.85	3.00	3.15
E2	1.635	1.735	1.835
H	0.41	0.56	0.71
K	0.585	0.685	0.785
L	0.30	0.40	0.50
L1	0.05	0.15	0.25
L2	-	-	0.15
$\theta$	8°	10°	12°

COMMON DIMENSIONS  
( UNITS OF MEASURE = MILLIMETER )