



Description

JMT N-channel Enhancement Mode Power MOSFET

Features

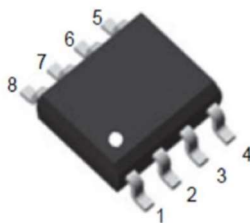
- 60V,17A
 $R_{DS(ON)} < 9m\Omega @ V_{GS} = 10V$
 $R_{DS(ON)} < 12m\Omega @ V_{GS} = 4.5V$
- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired

Application

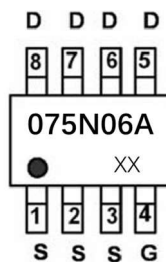
- Load Switch
- PWM Application
- Power management



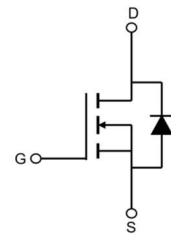
100% UIS TESTED!
100% ΔVds TESTED!



SOP-8 top view



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
075N06A	JMTP075N06A	TAPING	SOP-8	13inch	4000	48000

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Max.	Units
V_{DSS}	Drain-Source Voltage	60	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_A = 25^\circ\text{C}$	17
		$T_A = 100^\circ\text{C}$	11
I_{DM}	Pulsed Drain Current <small>note1</small>	68	A
EAS	Single Pulsed Avalanche Energy <small>note2</small>	140	mJ
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	4.8
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	26	$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$



Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	60	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} = 0V,	-	-	1.0	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.0	1.7	2.5	V
R _{DS(on)}	Static Drain-Source on-Resistance <small>note3</small>	V _{GS} =10V, I _D =15A	-	6.7	9	mΩ
		V _{GS} =4.5V, I _D =10A	-	8.5	12	
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	-	6276	-	pF
C _{oss}	Output Capacitance		-	300	-	pF
C _{rss}	Reverse Transfer Capacitance		-	262	-	pF
Q _g	Total Gate Charge	V _{DS} =30V, I _D =10A, V _{GS} =10V	-	98	-	nC
Q _{gs}	Gate-Source Charge		-	12.5	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	32	-	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DS} =30V, I _D =15A, R _G =1.8Ω, V _{GS} =10V	-	9	-	ns
t _r	Turn-on Rise Time		-	6.1	-	ns
t _{d(off)}	Turn-off Delay Time		-	33.2	-	ns
t _f	Turn-off Fall Time		-	7.5	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	17	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	68	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S =17A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	I _F =15A, di/dt=100A/μs	-	31	-	ns
Q _{rr}	Body Diode Reverse Recovery Charge		-	48	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition : T_J=25°C, V_{DD}=30V, V_G=10V, L=0.5mH, R_G=25Ω, I_{AS}=23.7A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%



Typical Performance Characteristics

Figure 1: Output Characteristics

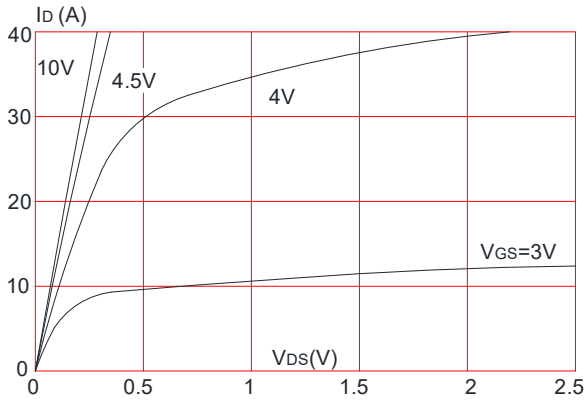


Figure 2: Typical Transfer Characteristics

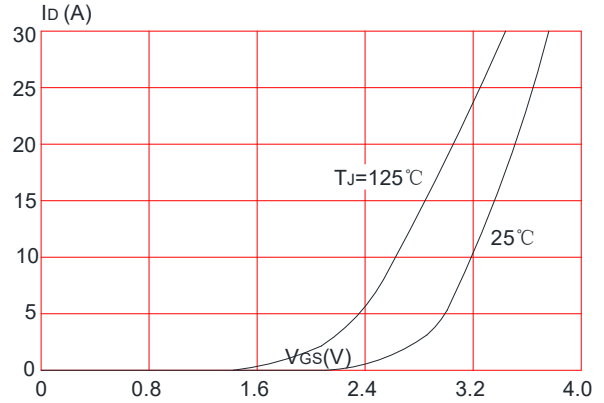


Figure 3: On-resistance vs. Drain Current

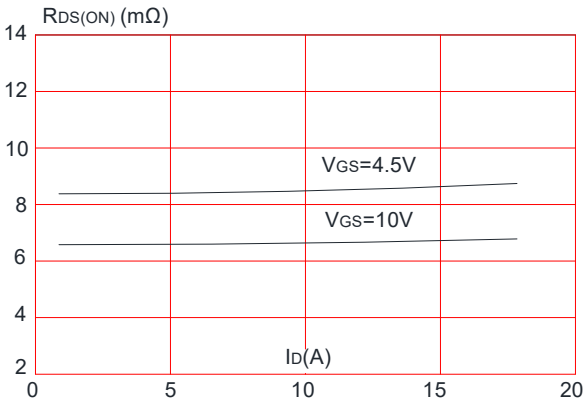


Figure 4: Body Diode Characteristics

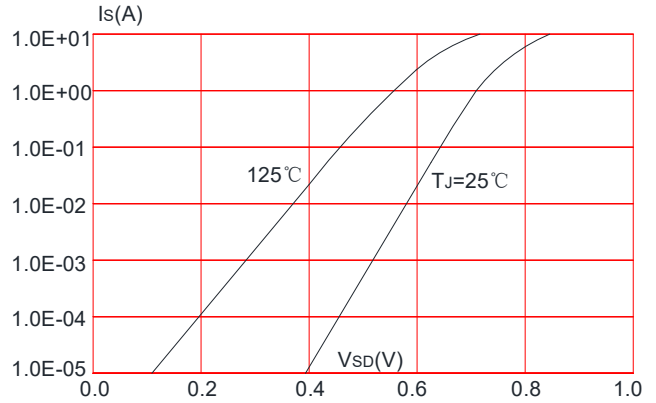


Figure 5: Gate Charge Characteristics

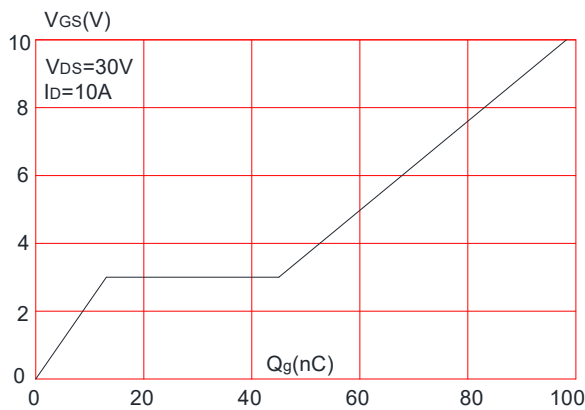


Figure 6: Capacitance Characteristics

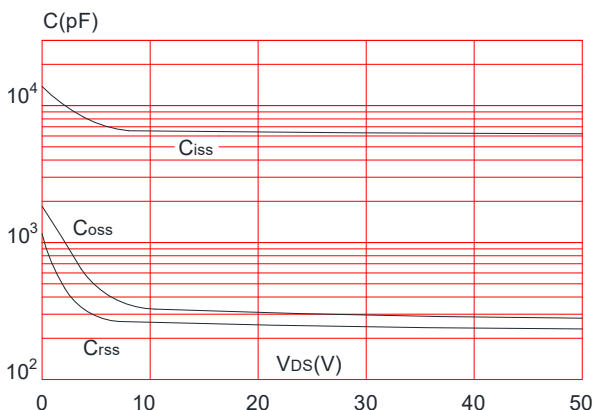




Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

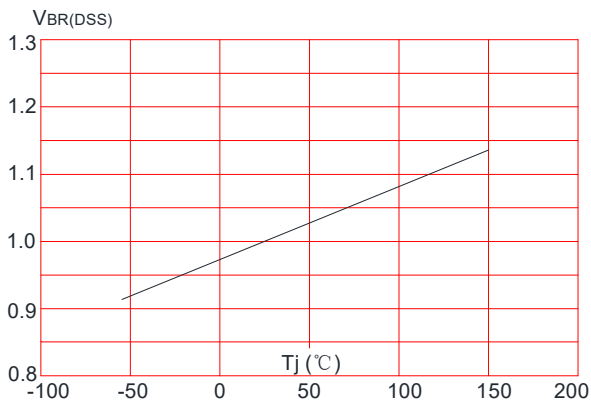


Figure 8: Normalized on Resistance vs. Junction Temperature

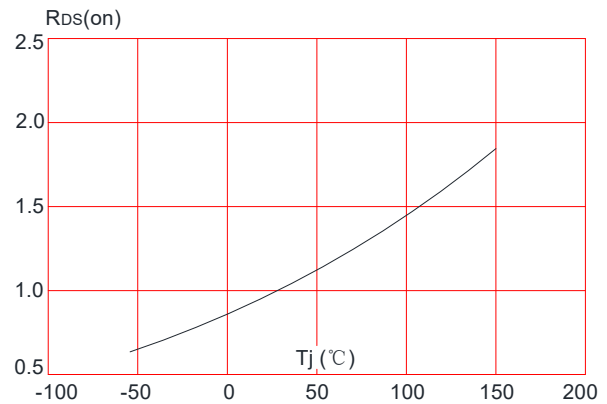


Figure 9: Maximum Safe Operating Area

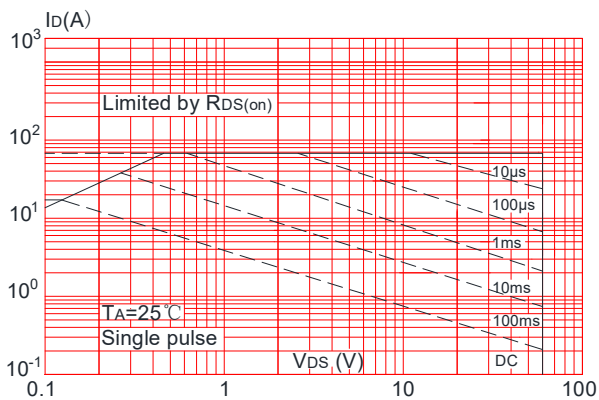


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

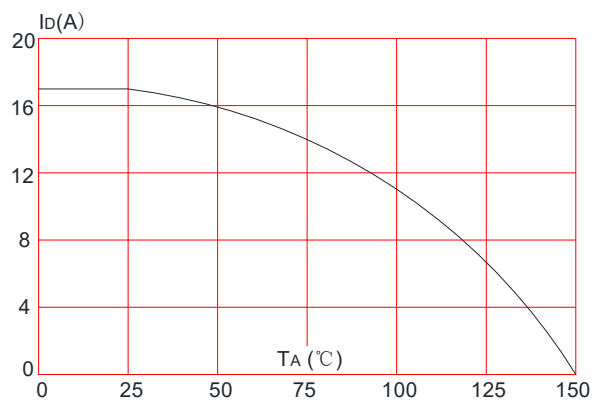
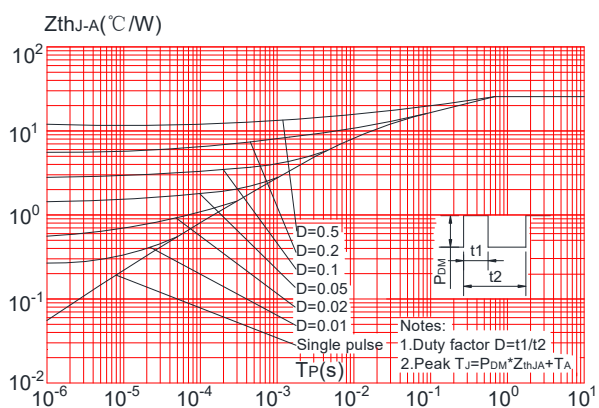


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



Test Circuit

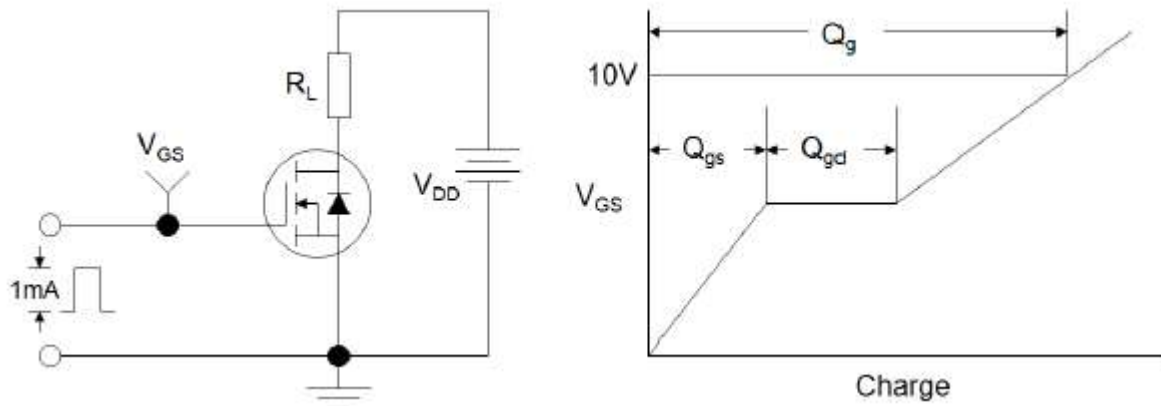


Figure 1: Gate Charge Test Circuit & Waveform

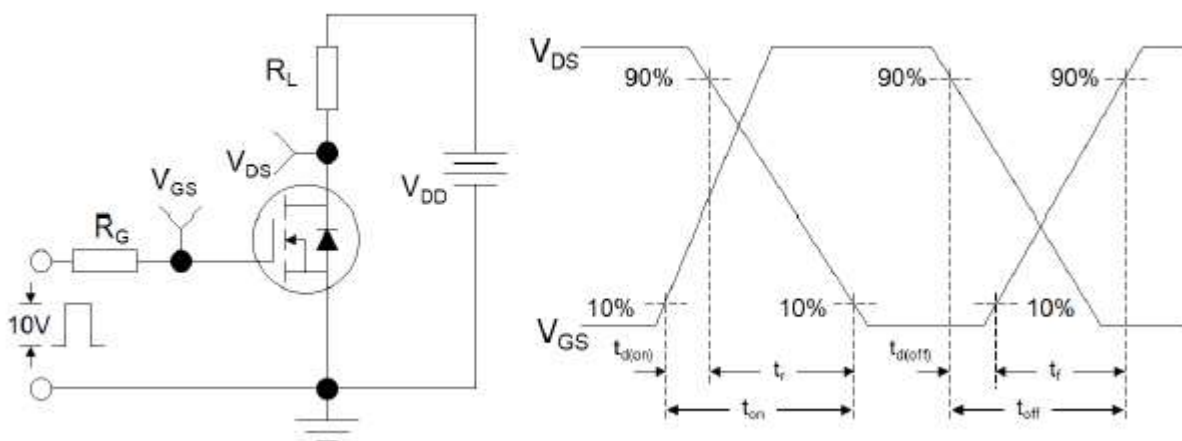


Figure 2: Resistive Switching Test Circuit & Waveforms

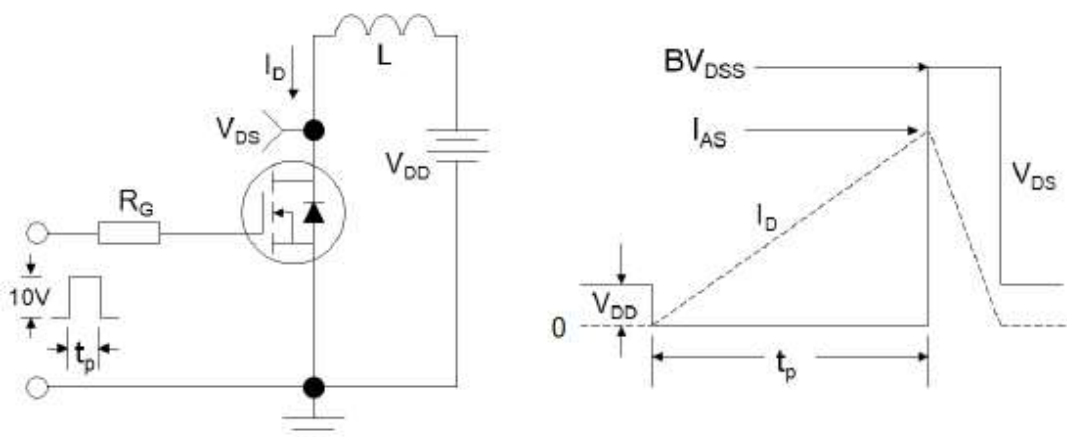
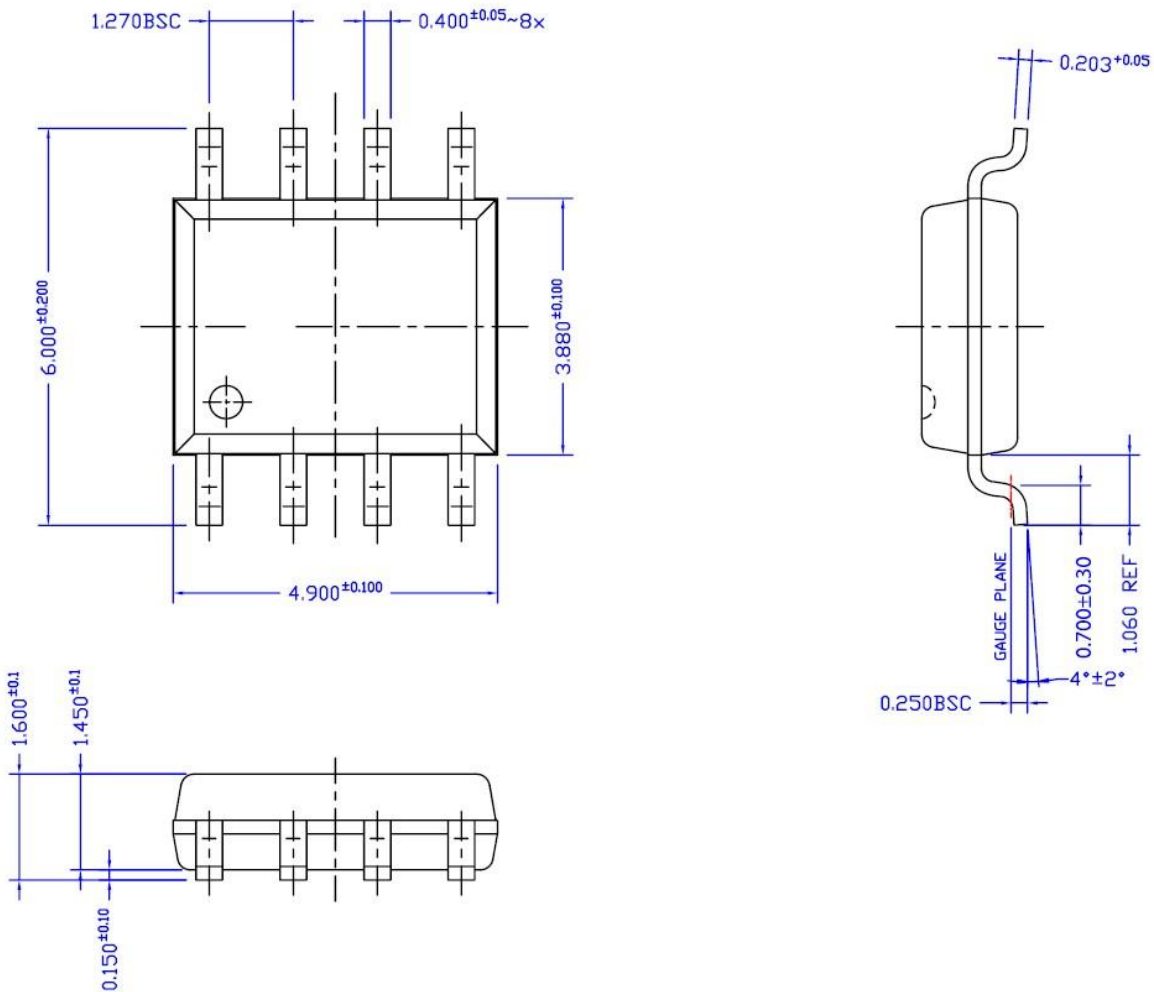


Figure 3: Unclamped Inductive Switching Test Circuit & Waveforms



Package Mechanical Data-SOP-8



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