



# JMTP170N06D

## Description

### JMT Dual N-channel Enhancement Mode Power MOSFET

#### Features

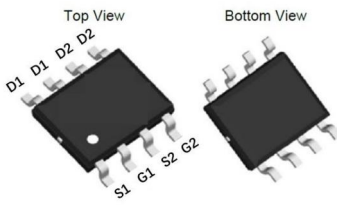
- 60V, 9.2A  
 $R_{DS(ON)} < 20.4m\Omega @ V_{GS} = 10V$   
 $R_{DS(ON)} < 24.4m\Omega @ V_{GS} = 4.5V$
- Advanced Trench Technology
- Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead Free

#### Application

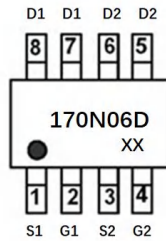
- Load Switch
- PWM Application
- Power Management



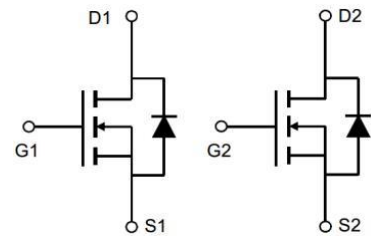
100% UIS TESTED!



SOP-8(Dual)



Marking and pin Assignment



Schematic Diagram

## Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel (pcs)	Per Carton (pcs)
170N06D	JMTP170N06D	TAPING	SOP-8	13"	4000	48000

## Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise specified)

Symbol	Parameter	Max.	Units
$V_{DSS}$	Drain-Source Voltage	60	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current	$T_A = 25^\circ C$	9.2
		$T_A = 100^\circ C$	6
$I_{DM}$	Pulsed Drain Current <sup>note1</sup>	36.8	A
EAS	Single Pulsed Avalanche Energy <sup>note2</sup>	64	mJ
$P_D$	Power Dissipation	$T_A = 25^\circ C$	1.19
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	105	$^\circ C/W$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$



## Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristics</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =60V, V <sub>GS</sub> = 0V,	-	-	1.0	μA
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.6	2.5	V
R <sub>DS(on)</sub>	Static Drain-Source on-Resistance <small>note3</small>	V <sub>GS</sub> =10V, I <sub>D</sub> =9A	-	16.3	20.4	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A	-	18.8	24.4	
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1.0MHz	-	2030	-	pF
C <sub>oss</sub>	Output Capacitance		-	130	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	115	-	pF
Q <sub>g</sub>	Total Gate Charge	V <sub>DD</sub> =30V, I <sub>D</sub> =5A, V <sub>GS</sub> =10V	-	46	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	7	-	nC
Q <sub>gd</sub>	Gate-Drain("Miller") Charge		-	10	-	nC
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> =30V, I <sub>D</sub> =5A, R <sub>GEN</sub> =1.8Ω, V <sub>GS</sub> =10V	-	9	-	ns
t <sub>r</sub>	Turn-on Rise Time		-	15	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time		-	36	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	6	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	9.2	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	36.8	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =9.2A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	I <sub>F</sub> =9A, di/dt=100A/μs	-	16	-	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge		-	13	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

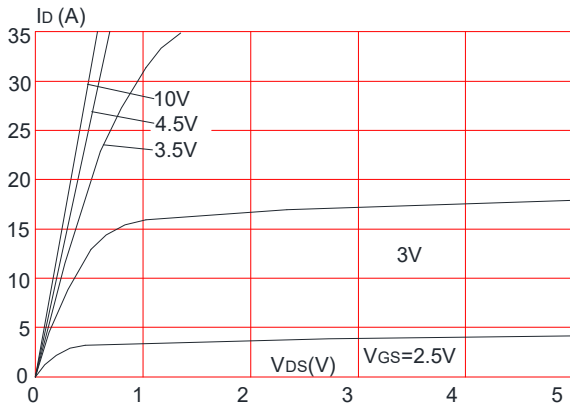
2. EAS condition : Starting T<sub>J</sub>=25°C, V<sub>DD</sub>=30V, V<sub>GS</sub>=10V, L=0.5mH, R<sub>g</sub>=25Ω, I<sub>AS</sub>=16A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

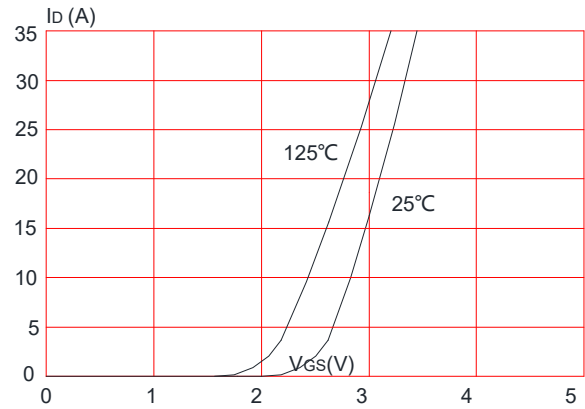


## Typical Performance Characteristics

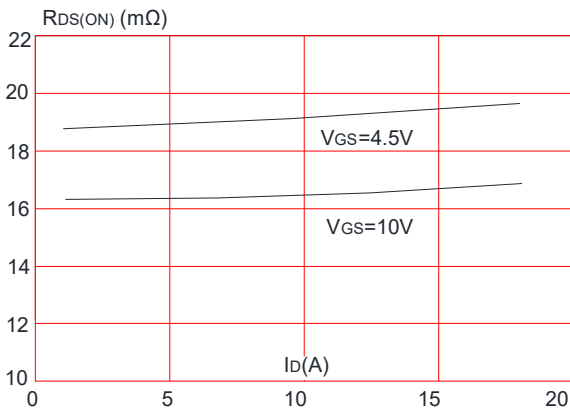
**Figure 1: Output Characteristics**



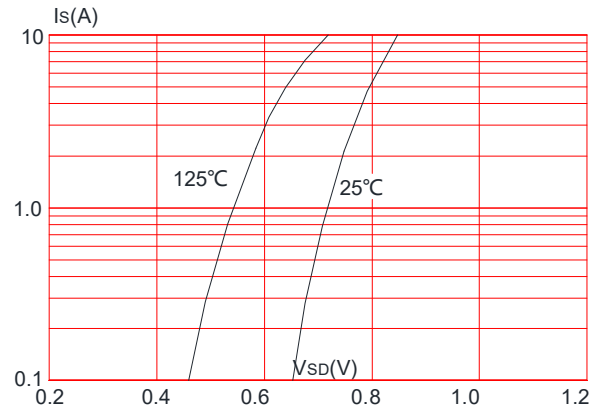
**Figure 2: Typical Transfer Characteristics**



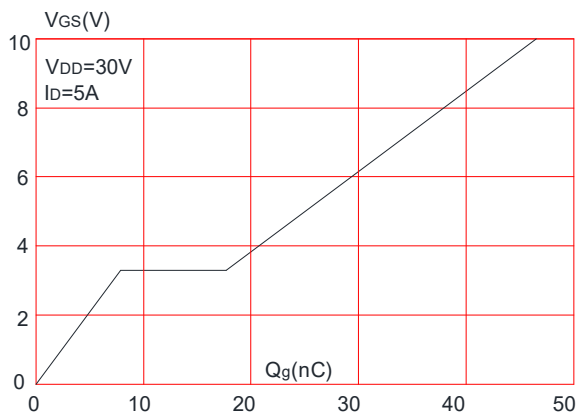
**Figure 3: On-resistance vs. Drain Current**



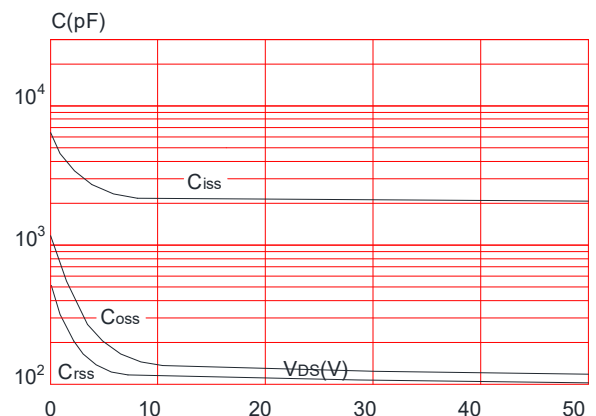
**Figure 4: Body Diode Characteristics**



**Figure 5: Gate Charge Characteristics**



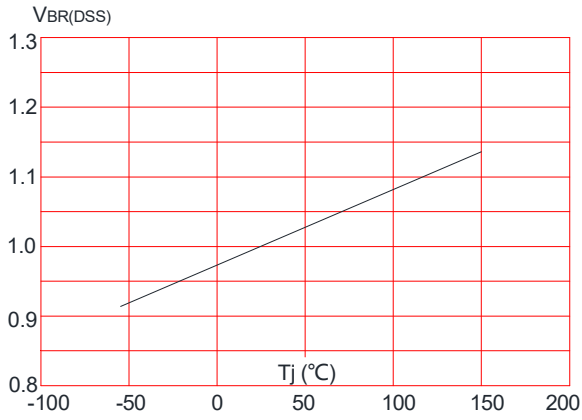
**Figure 6: Capacitance Characteristics**



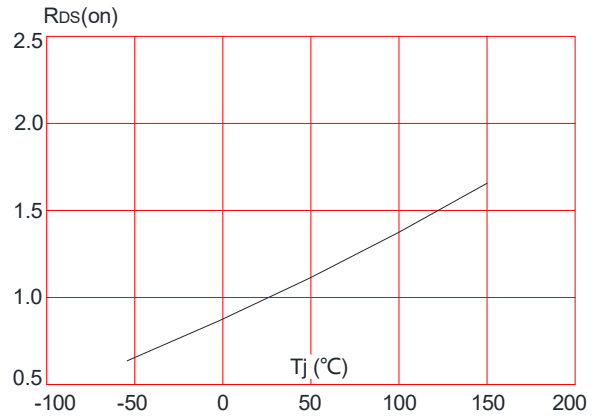


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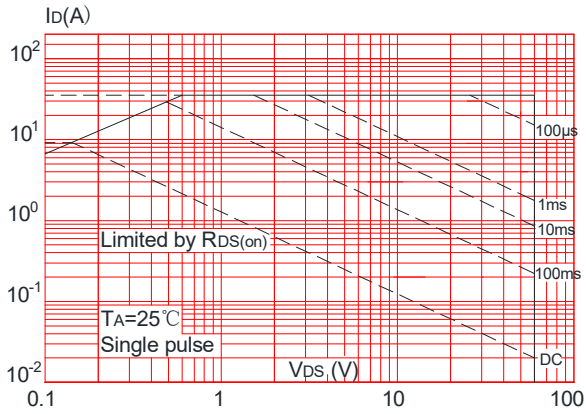
**Figure 7: Normalized Breakdown Voltage vs. Junction Temperature**



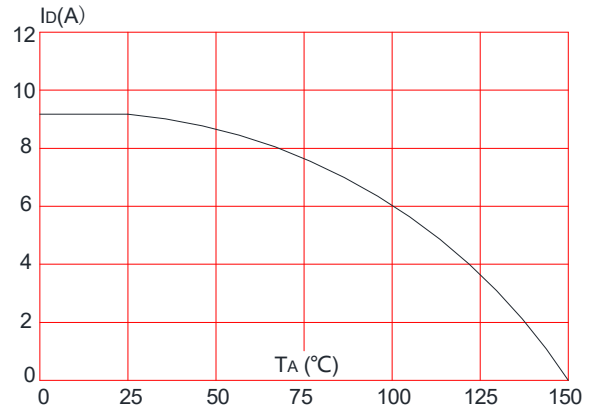
**Figure 8: Normalized on Resistance vs. Junction Temperature**



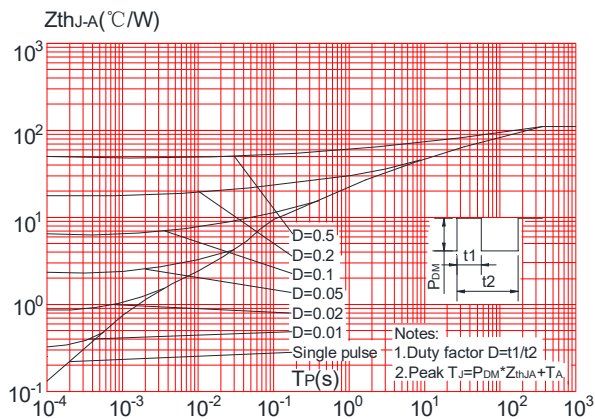
**Figure 9: Maximum Safe Operating Area**



**Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature**



**Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient**



## Test Circuit

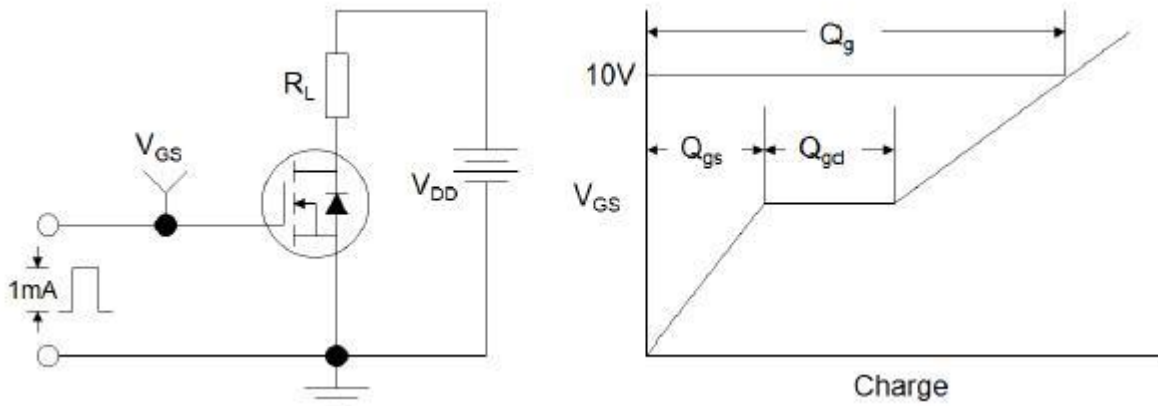


Figure1:Gate Charge Test Circuit & Waveform

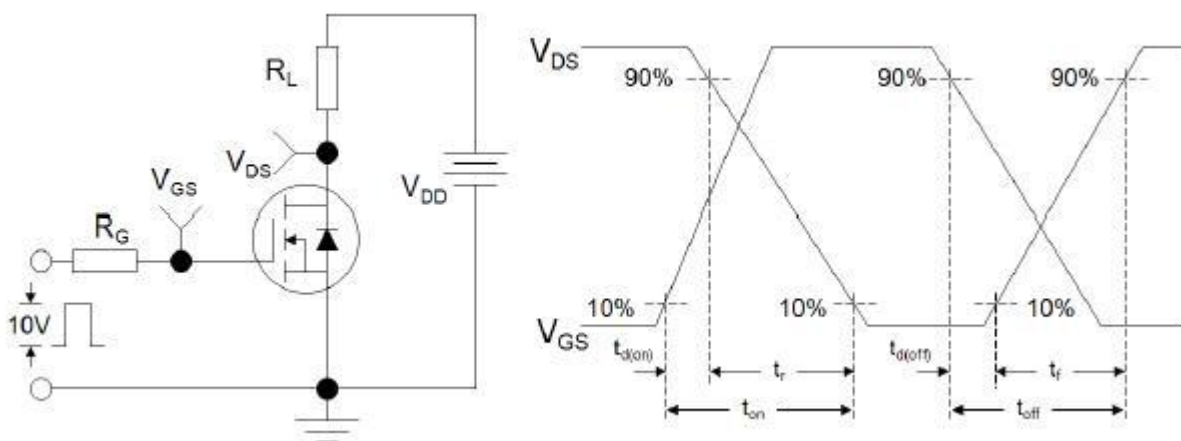


Figure 2: Resistive Switching Test Circuit & Waveforms

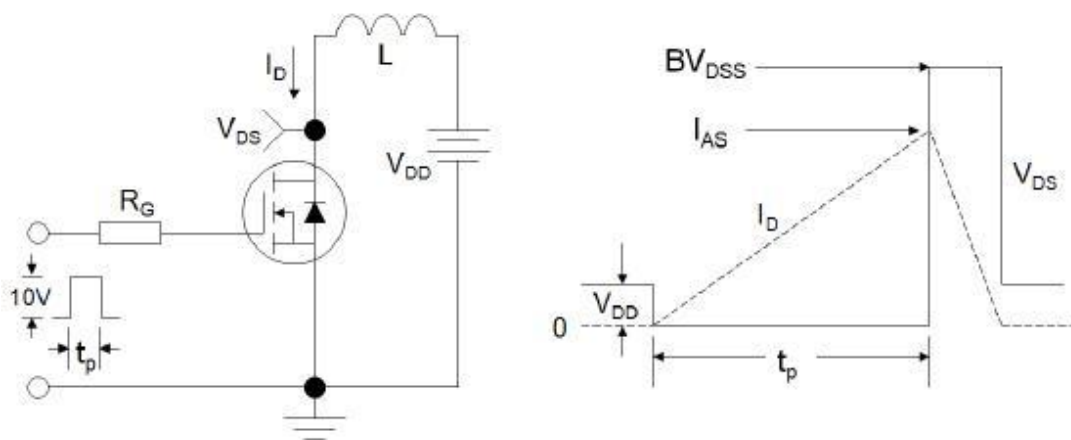
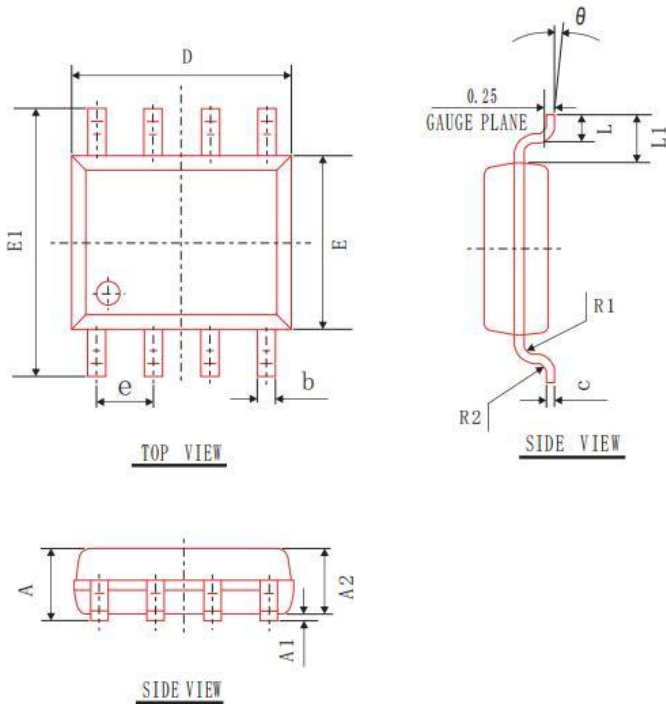


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



## Package Mechanical Data-SOP-8

COMMON DIMENSIONS  
(UNITS OF MEASURE=mm)



SYMBOL	MIN	NOM	MAX
A	1.40	1.60	1.80
A1	0.05	0.15	0.25
A2	1.35	1.45	1.55
b	0.30	0.40	0.50
c	0.153	0.203	0.253
D	4.80	4.90	5.00
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
L	0.45	0.70	1.00
$\theta$	2°	4°	6°
L 1	1.04 REF		
e	1.27 BSC		
R1	0.07 TYP		
R2	0.07 TYP		

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