650V GaN Power Transistor (FET)

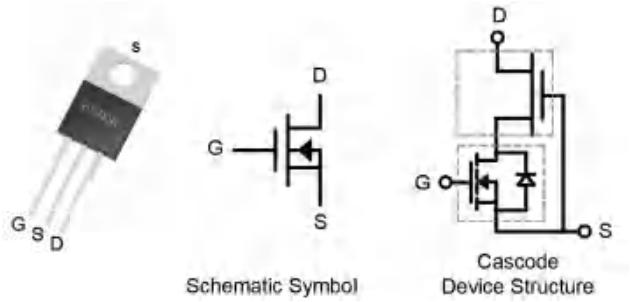
Features

- Easy to use, compatible with standard gate drivers
- Excellent Q_G x $R_{DS(on)}$ figure of merit (FOM)
- Low Q_{RR}, no free-wheeling diode required
- Low switching loss
- RoHS compliant and Halogen-free

Product Summary		
V_{DSS}	650	V
$R_{DS(on),\ typ}$	120	mΩ
$Q_{G,\ typ}$	21	nC
$Q_{RR,\ typ}$	26	nC

Applications

- High efficiency power supplies
- Telecom and datacom
- Automotive
- Servo motors



Packaging

Part Number	Package	Packaging	Base QTY
RX65T125PS2A	3 Lead TO-220	Tube	50

Maximum ratings, at T_C=25 °C, unless otherwise specified

Symbol	Parameter		Limit Value	Unit
I_D	Continuous drain current @T_C=25°C		23	A
	Continuous drain current @T_C=100°C		15	A
I_{DM}	Pulsed drain current @T_C=25°C (pulse width: 10us)		80	A
	Pulsed drain current @T_C=150°C (pulse width: 10us)		58	A
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)		650	V
V_{TDSS}	Transient drain to source voltage [a]		800	V
V_{GSS}	Gate to source voltage		±20	V
P_D	Maximum power dissipation @T_C=25°C		100	W
T_C	Operating temperature	Case	-55 to 150	°C
T_J		Junction	-55 to 150	°C
T_S	Storage temperature		-55 to 150	°C
T_{CSOLD}	Soldering peak temperature		260	°C

Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\Theta JC}$	Junction-to-case	1.25	°C/W
$R_{\Theta JA}$	Junction-to-ambient [b]	50	°C/W

Notes:

a. Off-state spike duty cycle < 0.01, spike duration < 2us

b. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm^2 copper area and 70μm thickness)

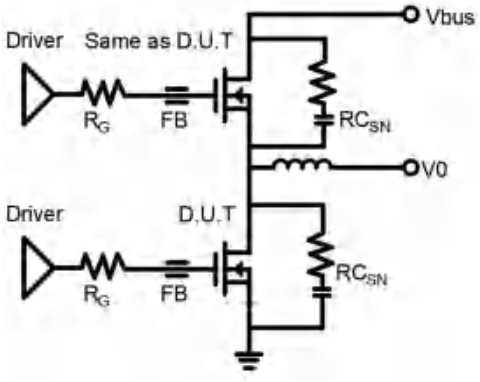
Electrical Parameters, at T_J=25 °C, unless otherwise specified

Symbol	Min	Typ	Max	Unit	Test Conditions
Forward Characteristics					
$V_{DSS-MAX}$	650	-	-	V	V_{GS}=0V
$V_{GS(th)}$	3.5	4	4.5	V	V_{DS}=V_{GS}, I_D=500μA
$R_{DS(on)}$ [c]	-	120	150	mΩ	V_{GS}=8V, I_D=4A, T_J=25°C
	-	240	-		V_{GS}=8V, I_D=4A, T_J=150°C
I_{DSS}	-	5	20	μA	V_{DS}=700V, V_{GS}=0V, T_J=25°C
	-	50	-	μA	V_{DS}=700V, V_{GS}=0V, T_J=150°C
I_{GSS}	-	-	150	nA	V_{GS}=20V
	-	-	-150	nA	V_{GS}=-20V
C_{ISS}	-	606	-	pF	V_{GS}=0V, V_{DS}=650V, f=1MHz
C_{OSS}	-	40	-	pF	
C_{RSS}	-	3	-	pF	
$C_{O(er)}$	-	57	-	pF	V_{GS}=0V, V_{DS}=0 - 650V
$C_{O(tr)}$	-	109	-	pF	
Q_G	-	21	-	nC	V_{DS}=400V, V_{GS}=0 - 12V, I_D=10A
Q_{GS}	-	6.7	-		
Q_{GD}	-	5	-		
$t_{D(on)}$	-	44	-	ns	V_{DS}=400V, V_{GS}=0 - 12V, I_D=10A, R_G=40Ω
t_R	-	16	-		
$t_{D(off)}$	-	40	-		
t_F	-	12	-		
Reverse Characteristics					
V_{SD}	-	1.3	-	V	V_{GS}=0V, I_S=5A, T_J=25°C
	-	1.9	-		V_{GS}=0V, I_S=10A, T_J=25°C
	-	3	-		V_{GS}=0V, I_S=10A, T_J=150°C
t_{RR}	-	16	-	ns	I_S=10A, V_{GS}=0V, d_i/d_t=1000A/us, V_{DD}=400V
Q_{RR}	-	26	-	nC	

Notes:

c. Dynamic on-resistance; see Figure 17 and 18 for test circuit and configurations

Circuit Implementation



Recommended Single Ended Drive Circuit

Recommended gate drive: (0 V, 12 V) with $R_{G(tot)}$ = 34 Ω, where $R_{G(tot)} = R_G + R_{Driver}$

Gate Ferrite Bead (FB)	Gate Resistance1 (R_G)	RC Snubber (RC_{SN})
MPZ1608S471ATA00	33 Ω	69 pF + 15 Ω

Notes:

d. RCsn should be placed as close as possible to the drain pin

e. The layout and wiring of the drive circuit should be as short as possible

Typical Characteristics, at T_C=25 °C, unless otherwise specified

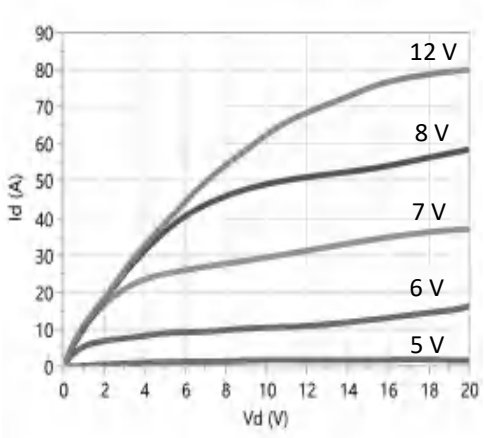


Figure 1. Typical Output Characteristics T_J=25°C

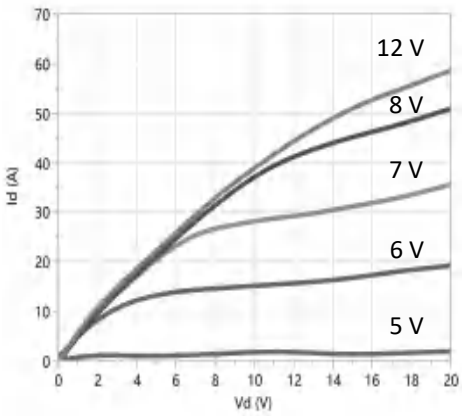


Figure 2. Typical Output Characteristics T_J=150°C

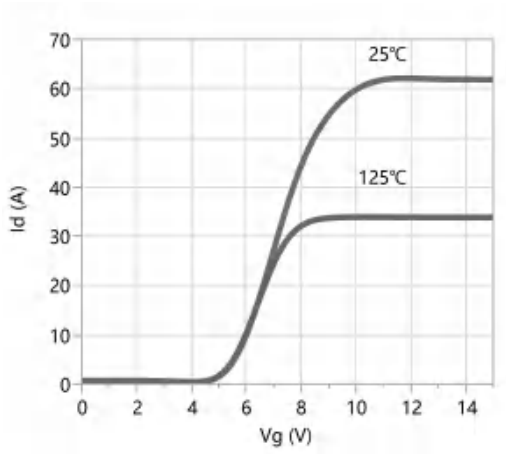


Figure 3. Typical Transfer Characteristics

V_{DS}=10V, Parameter: T_J

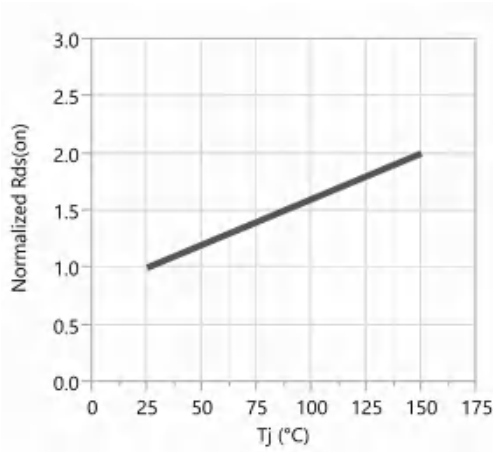


Figure 4. Normalized On-resistance

I_D=4A, V_{GS}=12V

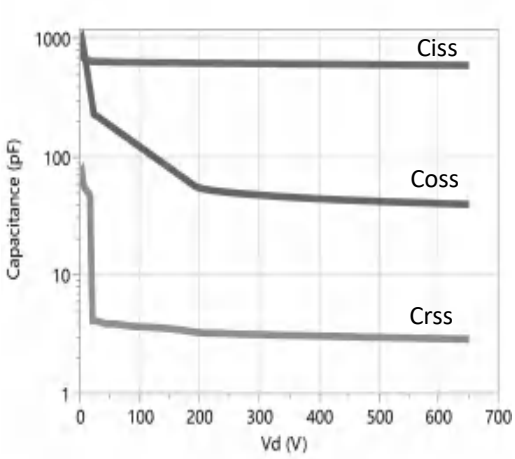


Figure 5. Typical Capacitance

V_{GS}=0V, f=1MHZ

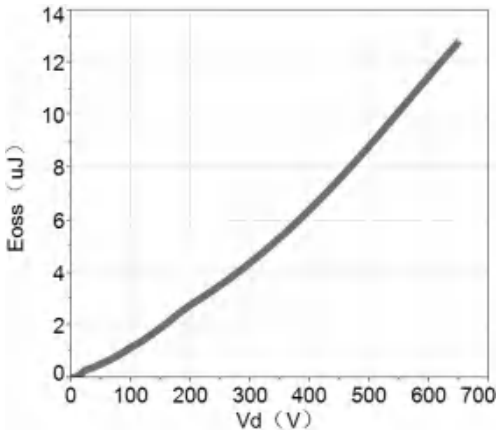


Figure 6. Typical Coss Stored Energy

Typical Characteristics, at T_C=25 °C, unless otherwise specified

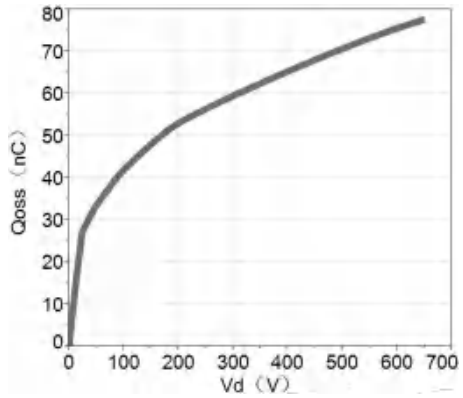


Figure 7. Typical Qoss

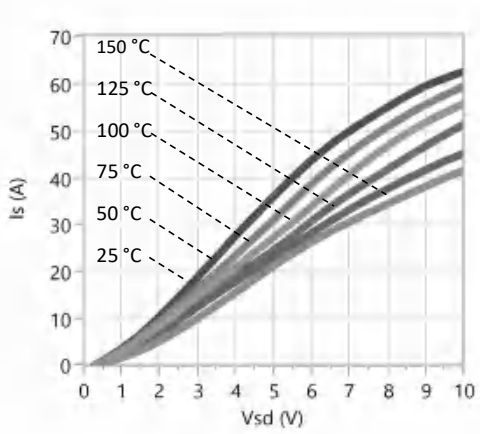


Figure 8. Forward Characteristic of Rev. Diode

$I_S=f(V_{Sd})$, Parameter: T_J

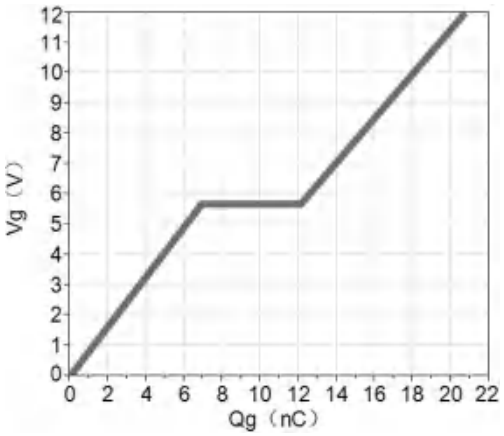


Figure 9. Typical Gate Charge

I_{DS}=10A, V_{DS}=400V

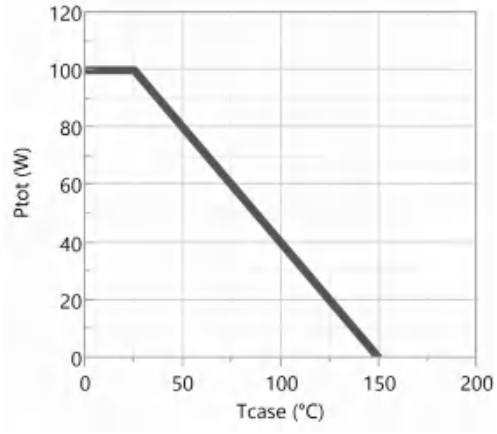


Figure 10. Power Dissipation

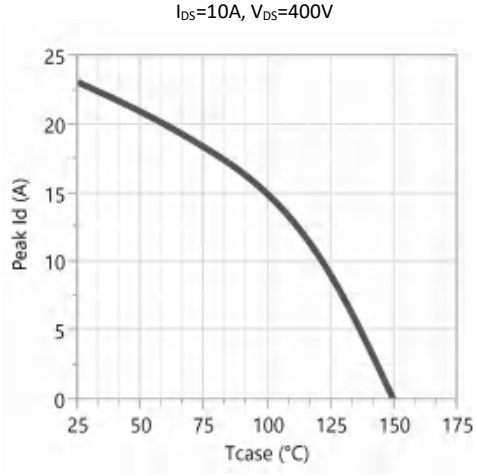


Figure 11. Current Derating

Typical Characteristics, at T_C=25 °C, unless otherwise specified

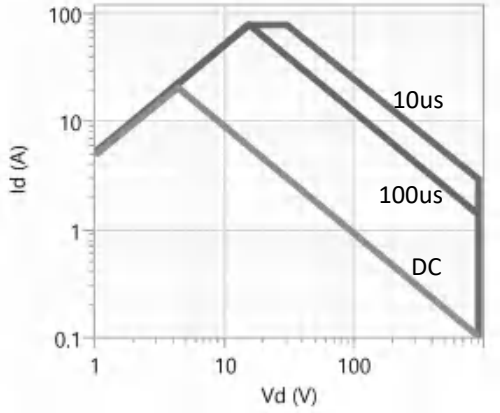


Figure 12. Safe operating Area T_C=25 °C

(calculated based on thermal limits)

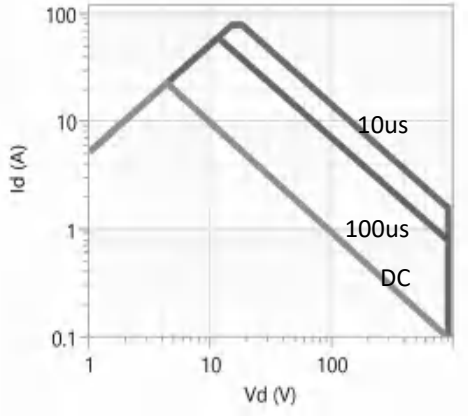


Figure 13. Safe operating Area T_C=80 °C

(calculated based on thermal limits)

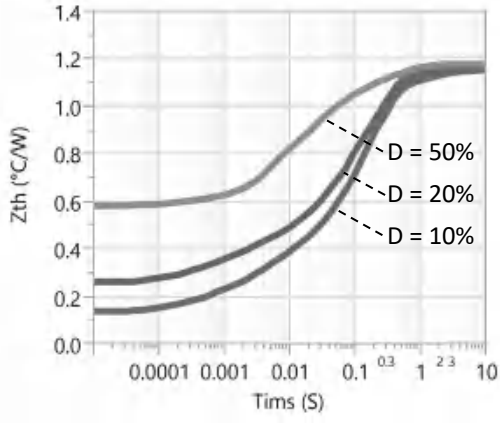


Figure 14. Transient Thermal Resistance

Test Circuits and Waveforms

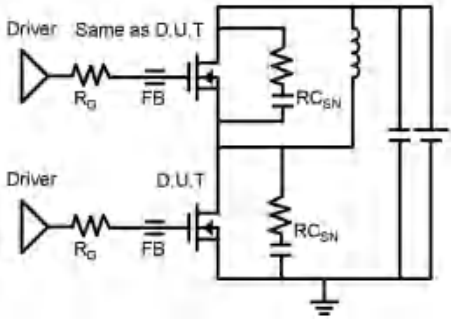


Figure 15. Switching Time Test Circuit

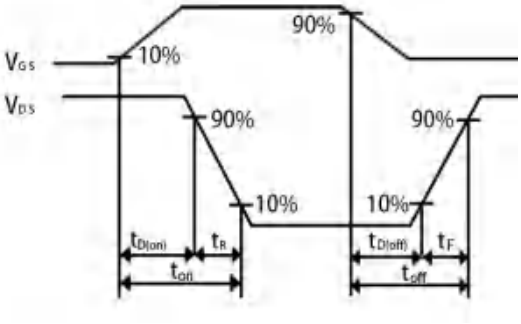


Figure 16. Switching Time Waveform

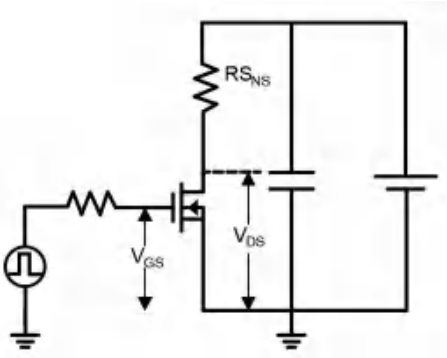


Figure 17. Dynamic $R_{DS(on)}$ Test Circuit

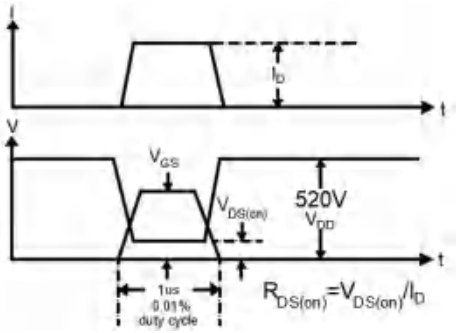


Figure 18. Dynamic $R_{DS(on)}$ Waveform

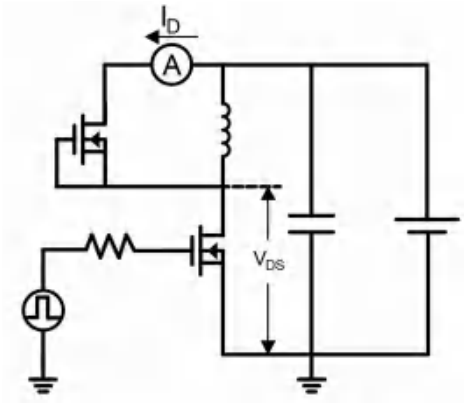


Figure 19. Diode Characteristic Test Circuit

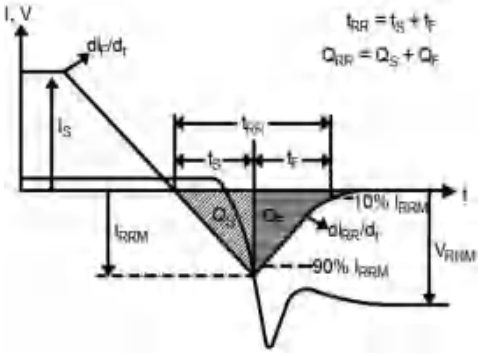


Figure 20. Diode Recovery Waveform

Design Considerations

Fast switching GaN device can reduce power conversion losses, and thus enable high frequency operations. Certain PCB design rules and instructions, however, need to be followed to take full advantages of fast switching GaN devices.

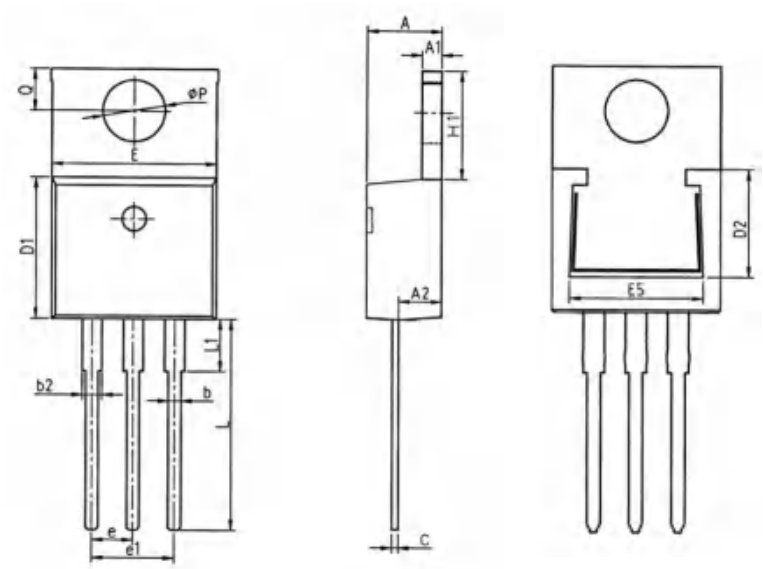
Before evaluating Runxin Micro's GaN devices, please refer to the table below which provides some practical rules that should be followed during the evaluation.

When Evaluating Runxin Micro's GaN Devices:

DO	DO NOT
Make sure the traces are as short as possible for both drive and power loops to minimize parasitic inductance	Using Runxin Micro's devices in GDS board layouts
Use the test tool with the shortest inductive loop, and make sure test points should be placed close enough	Use differential mode probe or probe ground clip with long wires
Minimize the lead length of TO packages when installing them to PCB	Use long traces in drive circuit, or long lead length of the devices

Package Outline

Pin 1: Gate; Pin 2: Source; Pin 3: Drain; Tab: Source

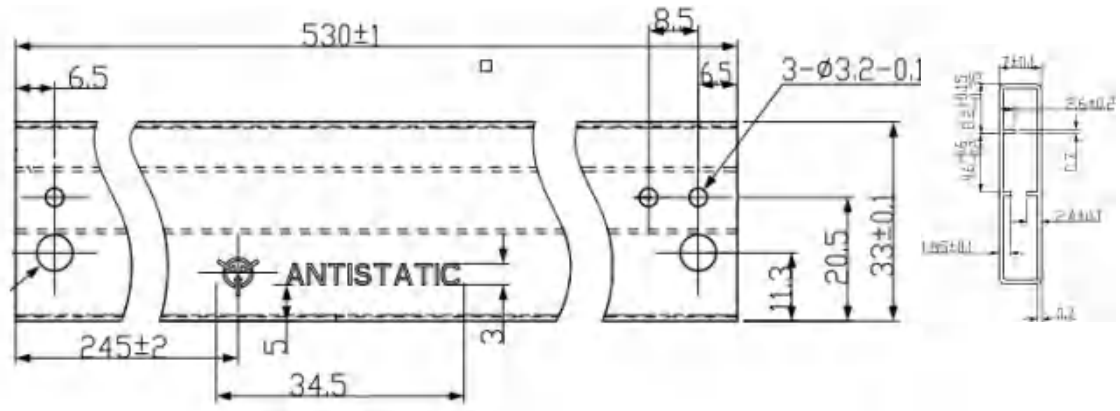


COMMON DIMENSIONS

SYMBOL	MM		
	MIN	NOM	MAX
A	4.37	4.57	4.77
A1	1.22	1.27	1.42
A2	2.49	2.69	2.89
b	0.75	0.81	0.96
b2	1.22	1.27	1.47
c	0.3	0.38	0.48
D1	8.5	8.7	8.9
D2	5.2	-	-
E	9.86	10.16	10.36
E5	7.06	-	-
e	2.54 BSC		
e1	5.08 BSC		
H1	6.1	6.3	6.5
L	13.1	13.4	13.7
L1	-	3.75	4.1
ΦP	3.7	3.84	3.99
Q	2.54	2.74	2.94

Tube Information

Dimensions are shown in millimeters



Revision History

Version	Date	Change(s)
1.0	10/29/2022	Release formal datasheet
1.1	11/03/2022	Revise $C_{O(er)}$ 、$C_{O(tr)}$、Q_G、Q_{GS}、Q_{GD}