

650V GaN Power Transistor (FET)

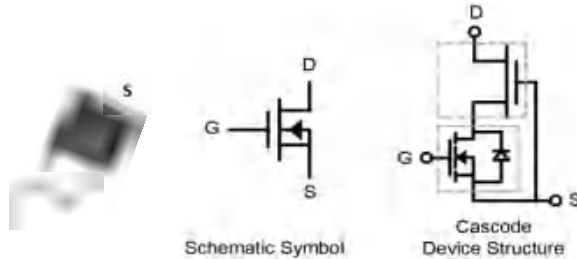
Features

- Easy to use, compatible with standard gate drivers
- Excellent $Q_G \times R_{DS(on)}$ figure of merit (FOM)
- Low Q_{RR} , no free-wheeling diode required
- Low switching loss
- RoHS compliant and Halogen-free

Product Summary		
V_{DSS}	650	V
$R_{DS(on), typ}$	240	m Ω
Q_G, typ	21	nC
$Q_{RR, typ}$	39	nC

Applications

- High efficiency power supplies
- Telecom and datacom
- Automotive
- Servo motors



Packaging

Part Number	Package	Packaging	Base QTY
RX65T300DS2A	2 Lead TO-252	Tape and Reel	2500

Maximum ratings, at $T_c=25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Limit Value	Unit
I_D	Continuous drain current @ $T_c=25^\circ\text{C}$	9	A
	Continuous drain current @ $T_c=100^\circ\text{C}$	5.5	A
I_{DM}	Pulsed drain current @ $T_c=25^\circ\text{C}$ (pulse width: 10us)	40	A
	Pulsed drain current @ $T_c=150^\circ\text{C}$ (pulse width: 10us)	26	A
V_{DSS}	Drain to source voltage ($T_J = -55^\circ\text{C}$ to 150°C)	650	V
V_{TDSS}	Transient drain to source voltage ^a	800	V
V_{GSS}	Gate to source voltage	± 20	V
P_D	Maximum power dissipation @ $T_c=25^\circ\text{C}$	40	W
T_C	Operating temperature	Case	-55 to 150 $^\circ\text{C}$
T_J		Junction	-55 to 150 $^\circ\text{C}$
T_S	Storage temperature	-55 to 150	$^\circ\text{C}$
T_{CSOLD}	Soldering peak temperature	260	$^\circ\text{C}$

Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Junction-to-case	3.1	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient ^b	50	$^{\circ}\text{C}/\text{W}$

Notes:

- a. Off-state spike duty cycle < 0.01 , spike duration $< 2\mu\text{s}$
- b. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm^2 copper area and $70\mu\text{m}$ thickness)

Electrical Parameters, at $T_J=25^\circ\text{C}$, unless otherwise specified

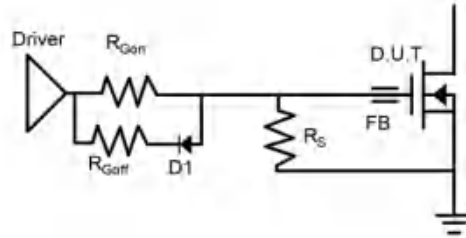
Symbol	Min	Typ	Max	Unit	Test Conditions
Forward Characteristics					
$V_{DSS-MAX}$	650	-	-	V	$V_{GS}=0V$
BV_{DSS}		1000			$V_{GS}=0V, I_{DSS}=250\mu A$
$V_{GS(th)}$	1.1	1.8	2.5	V	$V_{DS}=V_{GS}, I_D=500\mu A$
$R_{DS(on)}^c$	-	240	300	m Ω	$V_{GS}=8V, I_D=4A, T_J=25^\circ\text{C}$
	-	500	-		$V_{GS}=8V, I_D=4A, T_J=150^\circ\text{C}$
I_{DSS}	-	8	20	μA	$V_{DS}=700V, V_{GS}=0V, T_J=25^\circ\text{C}$
	-	50	-	μA	$V_{DS}=700V, V_{GS}=0V, T_J=150^\circ\text{C}$
I_{GSS}	-	-	150	nA	$V_{GS}=20V$
	-	-	-150	nA	$V_{GS}=-20V$
C_{ISS}	-	500	-	pF	$V_{GS}=0V, V_{DS}=650V, f=1\text{MHz}$
C_{OSS}	-	18	-	pF	
C_{RSS}	-	2	-	pF	
$C_{O(er)}$	-	25	-	pF	$V_{GS}=0V, V_{DS}=0 - 650V$
$C_{O(tr)}$	-	45	-	pF	
Q_G	-	21	-	nC	$V_{DS}=400V, V_{GS}=0 - 12V, I_D=5.5A$
Q_{GS}	-	3	-		
Q_{GD}	-	3.5	-		
$t_{D(on)}$	-	20	-	ns	$V_{DS}=400V, V_{GS}=0 - 12V, I_D=3A, R_G=30\Omega$
t_R	-	7	-		
$t_{D(off)}$	-	80	-		
t_F	-	6	-		
Reverse Characteristics					
V_{SD}	-	1.2	-	V	$V_{GS}=0V, I_S=2A, T_J=25^\circ\text{C}$
	-	1.7	-		$V_{GS}=0V, I_S=5A, T_J=25^\circ\text{C}$
	-	2	-		$V_{GS}=0V, I_S=5A, T_J=150^\circ\text{C}$
t_{RR}	-	12	-	ns	$I_S=3A, V_{GS}=0V, d_i/d_t=1000A/\mu s, V_{DD}=400V$
Q_{RR}	-	39	-	nC	

Notes:

C. Dynamic on-resistance; see Figure 17 and 18 for test circuit and configurations

Circuit Implementation

Mostly used in flyback, forward and push-pull converters



Recommended Single Ended Drive Circuit

Recommended gate drive: (0 V, 12 V) with $R_{Gon} = 300 - 500 \Omega$, $R_{Goff} = 10 \Omega$

Gate Ferrite Bead (FB)	Gate Resistance (R_{Gon})	Gate Resistance (R_{Goff})	Gate Source Resistance (R_S)	Gate Diode (D1)
300 - 600 Ω @100 MHz	300 - 500 Ω	10 Ω	10 k Ω	1N4148

Typical Characteristics, at $T_c=25\text{ }^\circ\text{C}$, unless otherwise specified

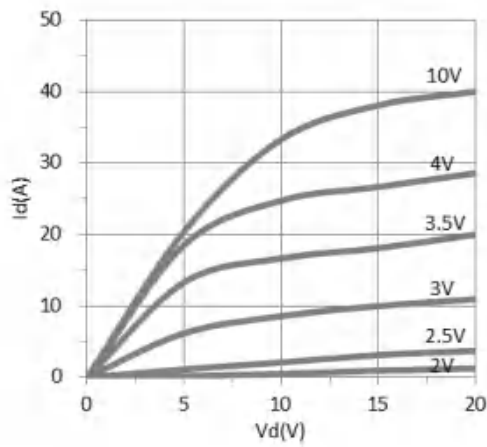


Figure 1. Typical Output Characteristics $T_j=25\text{ }^\circ\text{C}$

Parameter: V_{GS}

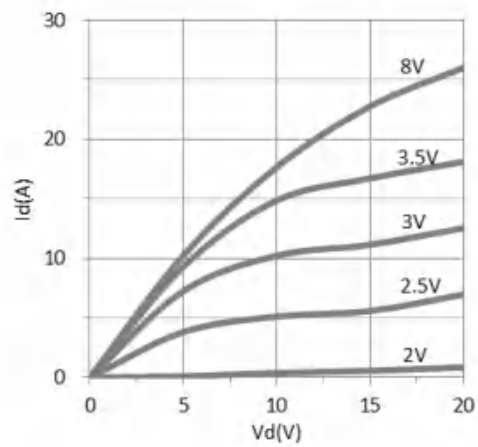


Figure 2. Typical Output Characteristics $T_j=150\text{ }^\circ\text{C}$

Parameter: V_{GS}

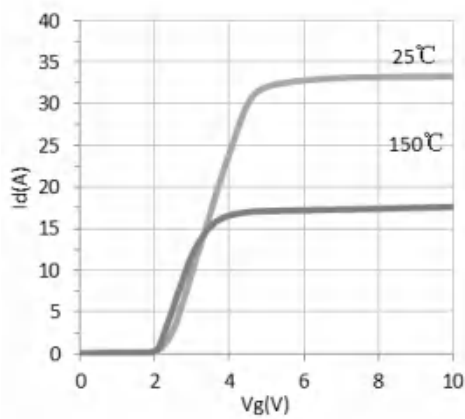


Figure 3. Typical Transfer Characteristics

$V_{DS}=10\text{V}$, Parameter: T_j

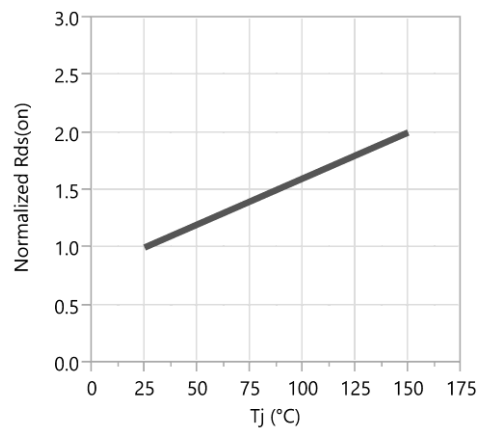


Figure 4. Normalized On-resistance

$I_D=4\text{A}$, $V_{GS}=8\text{V}$

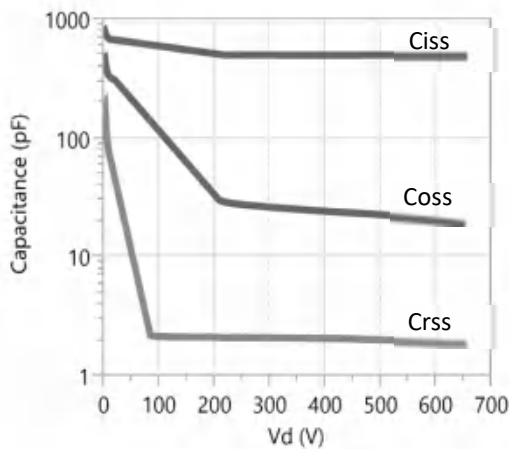


Figure 5. Typical Capacitance

$V_{GS}=0\text{V}$, $f=1\text{MHz}$

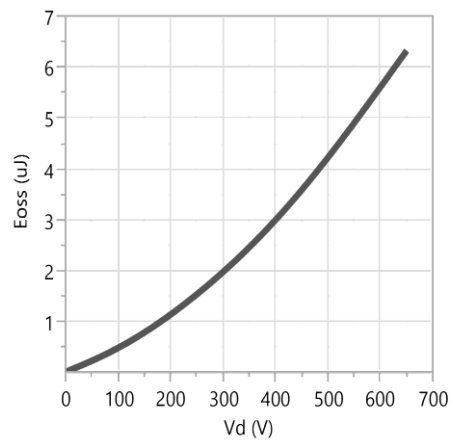


Figure 6. Typical C_{oss} Stored Energy

Typical Characteristics, at $T_c=25\text{ }^\circ\text{C}$, unless otherwise specified

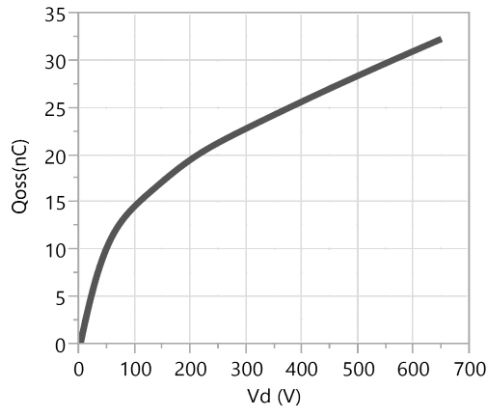


Figure 7. Typical Qoss

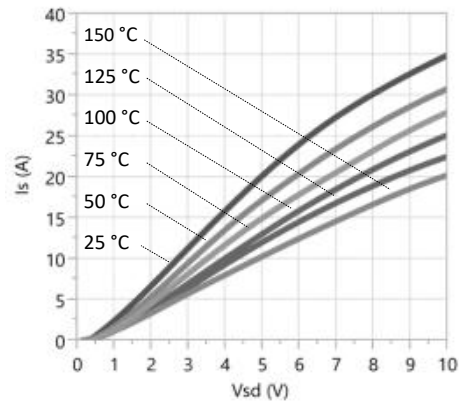


Figure 8. Forward Characteristic of Rev. Diode

$I_s=f(V_s)$, Parameter T_j

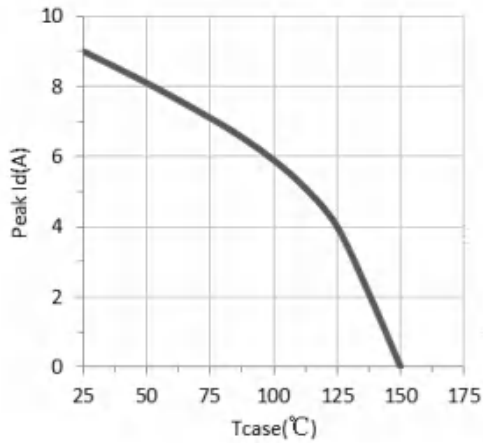


Figure 9. Current Derating

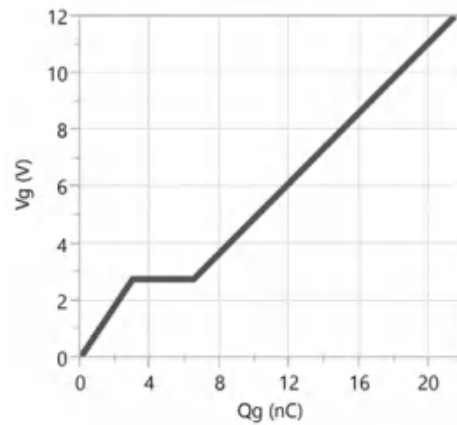


Figure 10. Typical Gate Charge

$I_{DS}=5.5\text{A}$, $V_{DS}=400\text{V}$

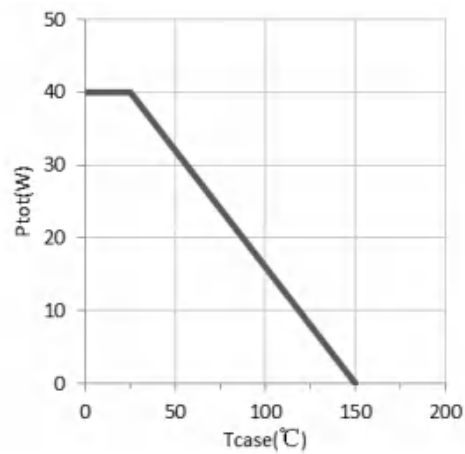


Figure 11. Power Dissipation

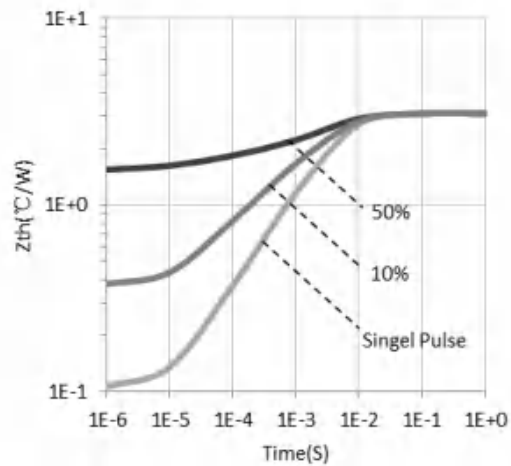


Figure 12. Transient Thermal Resistance

Typical Characteristics, at $T_c=25\text{ }^\circ\text{C}$, unless otherwise specified

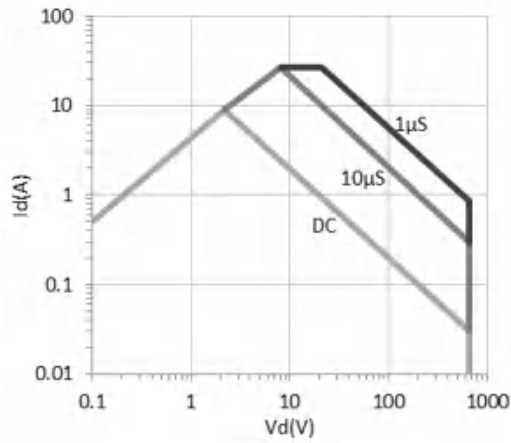


Figure 13. Safe operating Area $T_c=25\text{ }^\circ\text{C}$

(calculated based on thermal limits)

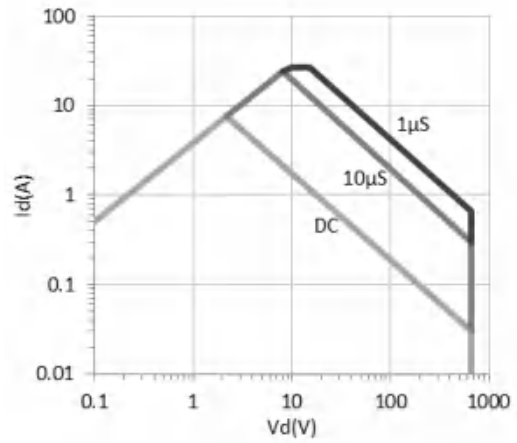


Figure 14. Safe operating Area $T_c=80\text{ }^\circ\text{C}$

(calculated based on thermal limits)

Test Circuits and Waveforms

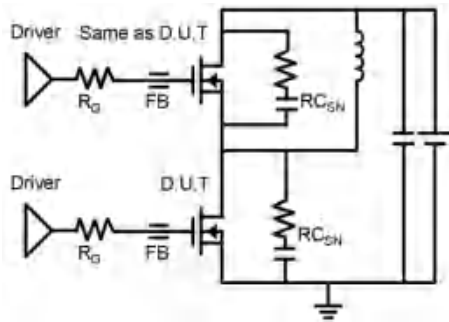


Figure 15. Switching Time Test Circuit

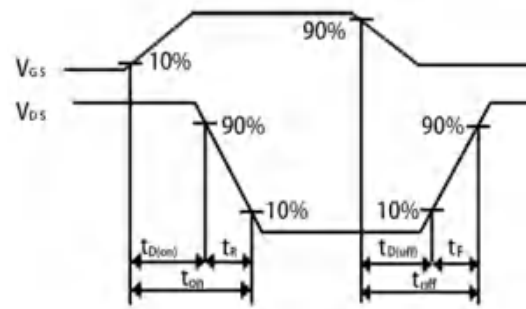


Figure 16. Switching Time Waveform

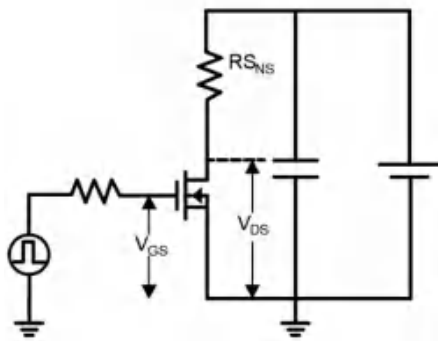


Figure 17. Dynamic $R_{DS(on)eff}$ Test Circuit

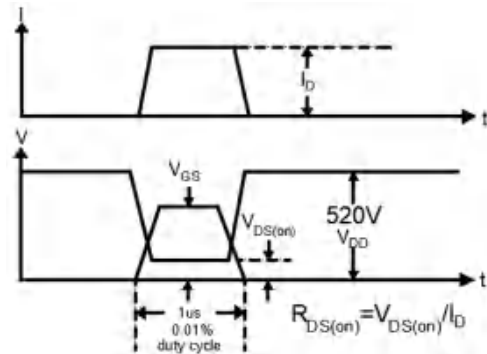


Figure 18. Dynamic $R_{DS(on)eff}$ Waveform

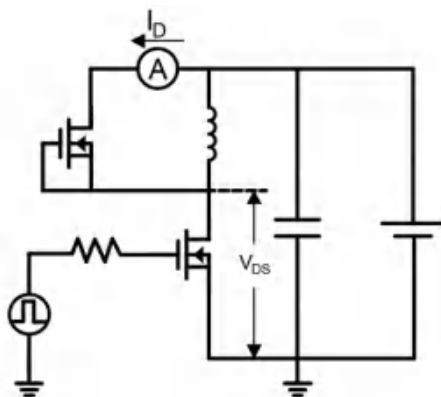


Figure 19. Diode Characteristic Test Circuits

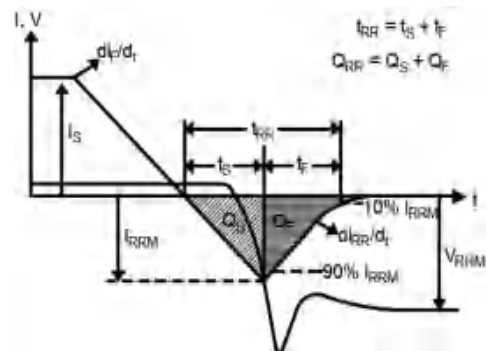


Figure 20. Diode Recovery Waveform

Design Considerations

Fast switching GaN device can reduce power conversion losses, and thus enable high frequency operations. Certain PCB design rules and instructions, however, need to be followed to take full advantages of fast switching GaN devices.

Before evaluating Runxin Micro's GaN devices, please refer to the table below which provides some practical rules that should be followed during the evaluation.

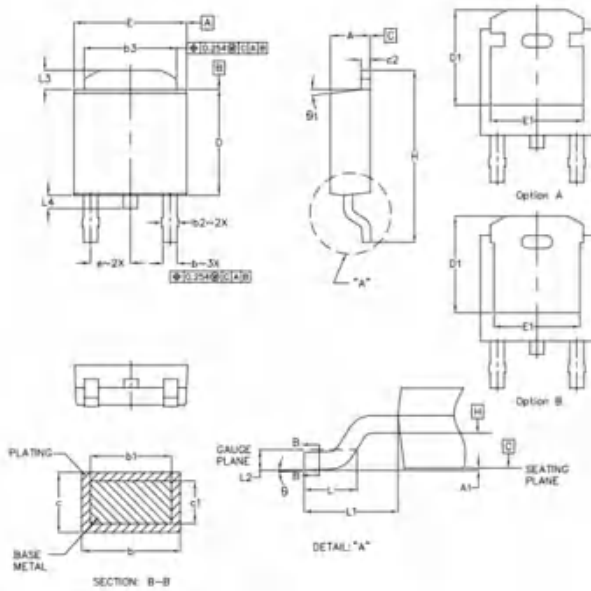
When Evaluating Runxin Micro's GaN Devices:

DO	DO NOT
Make sure the traces are as short as possible for both drive and power loops to minimize parasitic inductance	Using Runxin Micro's devices in GDS board layouts
Use the test tool with the shortest inductive loop, and make sure test points should be placed close enough	Use differential mode probe or probe ground clip with long wires
Minimize the lead length of TO packages when installing them to PCB	Use long traces in drive circuit, or long lead length of the devices

Package Outline

2 Lead TO-252 (DS) Package

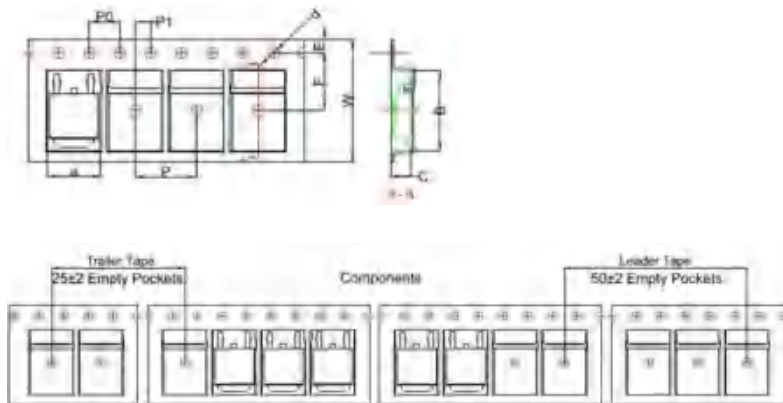
Pin 1: Gate; Pin 2: Drain; Tab: Source



Symbol	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.184	2.387	0.086	0.094
A1	—	0.127	—	0.005
b	0.750	0.890	0.029	0.035
b1	0.750	0.860	0.029	0.034
b2	0.762	1.143	0.030	0.046
b3	4.953	5.461	0.195	0.215
c	0.460	0.610	0.018	0.024
c1	0.410	0.559	0.016	0.022
-2	0.460	0.669	0.018	0.036
D	5.969	6.223	0.235	0.245
D1	5.207	—	0.205	—
E	6.350	6.731	0.250	0.265
E1	4.318	—	0.170	—
φ	2.290 BSC	—	0.090 BSC	—
H	9.595	10.414	0.375	0.410
L	1.397	1.778	0.055	0.070
L1	2.743 BSC	—	0.108 BSC	—
L2	0.508 BSC	—	0.020 BSC	—
L3	0.889	1.270	0.035	0.050
L4	—	1.016	—	0.040
θ	0°	10°	0°	10°
θ1	0°	15°	0°	15°

Tape Information

Dimensions are shown in millimeters



a	6.90±0.10
B	10.50±0.10
C	2.70±0.10
d	Φ1.50±0.10
E	1.75±0.10
E1	7.50±0.10
P0	1.00±0.10
P	5.00±0.10
P1	2.00±0.10
W	15.90-16.30

Revision History

Version	Date	Change(s)
0.1	03/02/2023	Release formal datasheet